LETTER

doi:10.1038/nature25494

Skin electronics from scalable fabrication of an intrinsically stretchable transistor array

Sihong Wang[1]*, Jie Xu[1]*, Weichen Wang[2], Ging-Ji Nathan Wang[1], Reza Rastak[3], Francisco Molina-Lopez[1], Jong Won Chung[1,4], Simiao Niu[1], Vivian R. Feig[2], Jeffery Lopez[1], Ting Lei[1], Soon-Ki Kwon[5], Yeongin Kim[6], Amir M. Foudeh[1], Anatol Ehrlich[1], Andrea Gasperini[1], Youngjun Yun[1,4], Boris Murmann[6], Jeffery B.-H. Tok[1] & Zhenan Bao[1]

Skin-like electronics that can adhere seamlessly to human skin or within the body are highly desirable for applications such as health monitoring[1,2], medical treatment[3,4], medical implants[5] and biological studies[6,7], and for technologies that include human–machine interfaces, soft robotics and augmented reality[8,9]. Rendering such electronics soft and stretchable—like human skin—would make them more comfortable to wear, and, through increased contact area, would greatly enhance the fidelity of signals acquired from the skin. Structural engineering of rigid inorganic and organic devices has enabled circuit-level stretchability, but this requires sophisticated fabrication techniques and usually suffers from reduced densities of devices within an array[2,10–12]. We reasoned that the desired parameters, such as higher mechanical deformability and robustness, improved skin compatibility and higher device density, could be provided by using intrinsically stretchable polymer materials instead. However, the production of intrinsically stretchable materials and devices is still largely in its infancy[13–15]: such materials have been reported[11,16–19], but functional, intrinsically stretchable electronics have yet to be demonstrated owing to the lack of a scalable fabrication technology. Here we describe a fabrication process that enables high yield and uniformity from a variety of intrinsically stretchable electronic polymers. We demonstrate an intrinsically stretchable polymer transistor array with an unprecedented device density of 347 transistors per square centimetre. The transistors have an average charge-carrier mobility comparable to that of amorphous silicon, varying only slightly (within one order of magnitude) when subjected to 100 per cent strain for 1,000 cycles, without current–voltage hysteresis. Our transistor arrays thus constitute intrinsically stretchable skin electronics, and include an active matrix for sensory arrays, as well as analogue and digital circuit elements. Our process offers a general platform for incorporating other intrinsically stretchable polymer materials, enabling the fabrication of next-generation stretchable skin electronic devices.

Electronics on human skin generally comprise, but are not limited to, two types of component: input/output devices for human interaction (the input might be, for example, a sensor element; the output might be a display), and electronic circuits for information processing. So far, stretchability has been demonstrated for certain input/output devices[20–24], but there are still no functional skin-like stretchable circuits, mostly because of the much higher complexity required at both circuit and device levels. Therefore, realizing skin electronics will rely on the development of intrinsically stretchable circuits composed of densely integrated transistors.

Fabricating intrinsically stretchable electronics (Fig. 1a) requires intrinsically stretchable materials, especially stretchable semiconductors and conductors that possess uncompromised electrical conduction, even under large strains. Recently, polymers have been shown to be the most promising materials family for enabling both high electrical performance and intrinsic stretchability[11,16–19]. Moving forwards, a fabrication technology is needed that incorporates these materials into mass-producible arrays of transistors. However, polymer-based intrinsically stretchable electronic materials are solution deposited, and are highly susceptible to damage from both organic solvents and ultraviolet light. In general, they are incompatible with standard photolithography microfabrication technology, making it highly challenging to produce functional electronics *en masse* beyond individual transistors. Another obstacle lies in the incorporation of new materials, which typically necessitates an entirely new fabrication process. Therefore, a universal fabrication process or platform for generating intrinsically stretchable transistor arrays is needed to move materials development systematically to electronics and, finally, to desired applications. Here, we describe a fabrication platform with high yield and uniformity, which results in intrinsically stretchable transistor arrays (Fig. 1a) with a density and device count that greatly surpass those achieved by strain engineering and other approaches (Extended Data Table 1). Highlighting its versatility, we use this platform to demonstrate various intrinsically stretchable electronics ranging from active matrices to analogue and digital circuits. Further integrating these circuit components together with stretchable input/output devices could finally bring about skin electronic systems.

With its stretchability enabled by intrinsically stretchable materials—rather than through geometry design with rigid materials—our fabricated stretchable transistor array (Fig. 1b) has a record transistor density of about 347 transistors per square centimetre, and has high stretchability (up to 100% while maintaining a charge-carrier mobility of 0.98 $cm^2 V^{-1} s^{-1}$). Moreover, the fabrication process can be scaled to produce a large array of 6,300 transistors over an area of around $4.4 \times 4.4\,cm^2$ (Fig. 1c); this array is semi-transparent and has skin-like conformability and stretchability. This transistor array platform has enabled the first realization of skin-like intrinsically stretchable circuits (Fig. 1d), as the basic components of skin electronics.

The general fabrication process flow is designed to enable high device yield, device-to-device uniformity, good material compatibility between layers, and good electrical and mechanical performances. Specifically, the process flow (Fig. 2a) uses layer-by-layer direct deposition of active components to avoid the low yield and poor uniformity typically obtained from transfer processes that rely on peeling off through physical adhesion. First, to ensure good substrate compatibility during all the fabrication processes, we begin with a silicon wafer that is coated with a water-soluble sacrificial layer (dextran) to enable final release of the devices onto a stretchable substrate. Next, a stretchable dielectric is deposited and photo-patterned. Then, a stretchable

[1]Department of Chemical Engineering, Stanford University, Stanford, California 94305, USA. [2]Department of Materials Science and Engineering, Stanford University, Stanford, California 94305, USA. [3]Department of Civil and Environmental Engineering, Stanford University, Stanford, California 94305, USA. [4]Samsung Advanced Institute of Technology, Yeongtong-gu, Suwon-si, Gyeonggi-do 443-803, Republic of Korea. [5]Department of Materials Engineering and Convergence Technology and ERI, Gyeongsang National University, Jinju, 660-701, Republic of Korea. [6]Department of Electrical Engineering, Stanford University, Stanford, California 94305, USA.
*These authors contributed equally to this work.

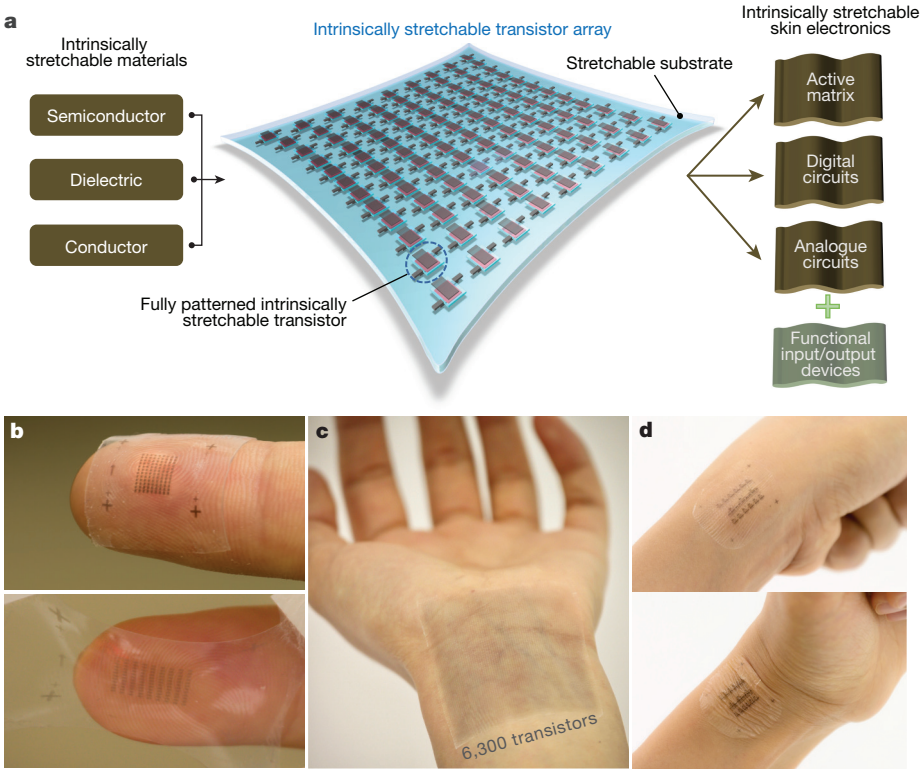


Figure 1 | Intrinsically stretchable transistor array as a core platform for functional skin electronics. a, Three-dimensional diagram of an intrinsically stretchable transistor array as the core building block of skin electronics. **b**, An array of 108 stretchable transistors on a fingertip, showing an unprecedented device density of 347 transistors per cm^2. **c**, A large-scale array of intrinsically stretchable transistors—with 6,300 transistors in an area of around $4.4 \times 4.4\,cm^2$—attached conformably to a human inner wrist. **d**, Intrinsically stretchable circuits—a prototype for highly conformable functional skin electronics—attached to a bent human wrist.

semiconductor and a stretchable conductor for source/drain electrodes (together with the first layer of interconnect) are deposited and patterned consecutively, to get a top-contact structure. A stretchable substrate is laminated onto the device, which is then soaked in water to release it from the rigid substrate. Finally, the gate electrodes (and the second layer of interconnect) are deposited and patterned on the dielectric layer to complete the transistor structure.

Below we discuss the key fabrication steps in greater detail. First, the photo-patterned dielectric layer (Extended Data Fig. 1) needs to be solvent resistant to allow semiconductor deposition. To realize this with general applicability to stretchable dielectrics, we took advantage of azide-crosslinking chemistry[25,26], which can be initiated by ultraviolet light, and which is based on a reaction between azide groups and the CH group that is commonly found in elastomers (Fig. 2b and Supplementary Fig. 1). The optimized patterning protocol (Supplementary Fig. 2) is applied to both polystyrene-*block*-poly(ethylene-*ran*-butylene)-*block*-polystyrene (SEBS) (Extended Data Fig. 2 and Supplementary Figs 3, 4) and polyurethane (Supplementary Fig. 5), with solvent resistance achieved afterwards.

Next, in order to pattern stretchable semiconductors, which are usually incompatible with traditional photolithography processes, we developed two strategies. The first is based on an etching process that involves protection by a copper mask, using a fluorinated polymer[27] as the sacrificial layer, the solvent for which will not dissolve other existing components of the device (Fig. 2c and Extended Data Fig. 3). In separating the film deposition from the patterning process, this method should be universally applicable to various stretchable semiconductors without sacrificing electrical performance (Extended Data Fig. 4). The second strategy uses inkjet printing[28] as an additive patterning method for large-scale fabrication (Fig. 2d and Extended Data Fig. 5), and is applicable to polymer semiconductors that show good solubility.

Using these processes, we fabricated a sheet comprising an intrinsically stretchable array of 108 transistors (Figs 1b and 2e, f), using crosslinked SEBS as the dielectric, a 'conjugated polymer/elastomer phase separation induced elasticity' (CONPHINE) film[16] (patterned by the etching method) as the semiconductor, and carbon nanotubes[22] (spray-coated onto the device through shadow masks—thin metal plates with openings to generate patterns) as the electrodes (Supplementary Fig. 6). Here, to enable higher mobility, we modified the surface energy of the patterned SEBS dielectric layer to obtain the desirable CONPHINE film morphology (Extended Data Fig. 6). As shown in Fig. 2f, the transistors occupied most of the area and achieved a rather high density of 347 per cm^2. In a magnified image of one transistor in the array (Fig. 2g), all of the fully patterned and well aligned components can be clearly seen.

Our intrinsically stretchable transistor array devices show ideal switching behaviour, with no current hysteresis, an on/off current ratio as high as 10^4, minimal gate leakage (Fig. 3a and Supplementary Fig. 7), and good on-shelf and bias stabilities (Supplementary Fig. 8). Furthermore, low-voltage operation at around 10 V (Supplementary Fig. 10) makes the devices suitable for on-skin applications. An overall yield of 94.4% and high performance uniformity (Fig. 3b and Supplementary Fig. 11) were achieved for the 108-transistor array, even though it was fabricated in a non-clean-room environment (with just six transistors out of these 108 failing, owing to leakage of the dielectric layer). The charge-carrier mobilities from all of the working devices show a narrow distribution (Fig. 3c), with an average of $0.821 \pm 0.105\,cm^2\,V^{-1}\,s^{-1}$, and the highest value reaching $1.11\,cm^2\,V^{-1}\,s^{-1}$. For a less-dense array with a larger channel length (110 μm), the mobility is even higher (average $1.37\,cm^2\,V^{-1}\,s^{-1}$;

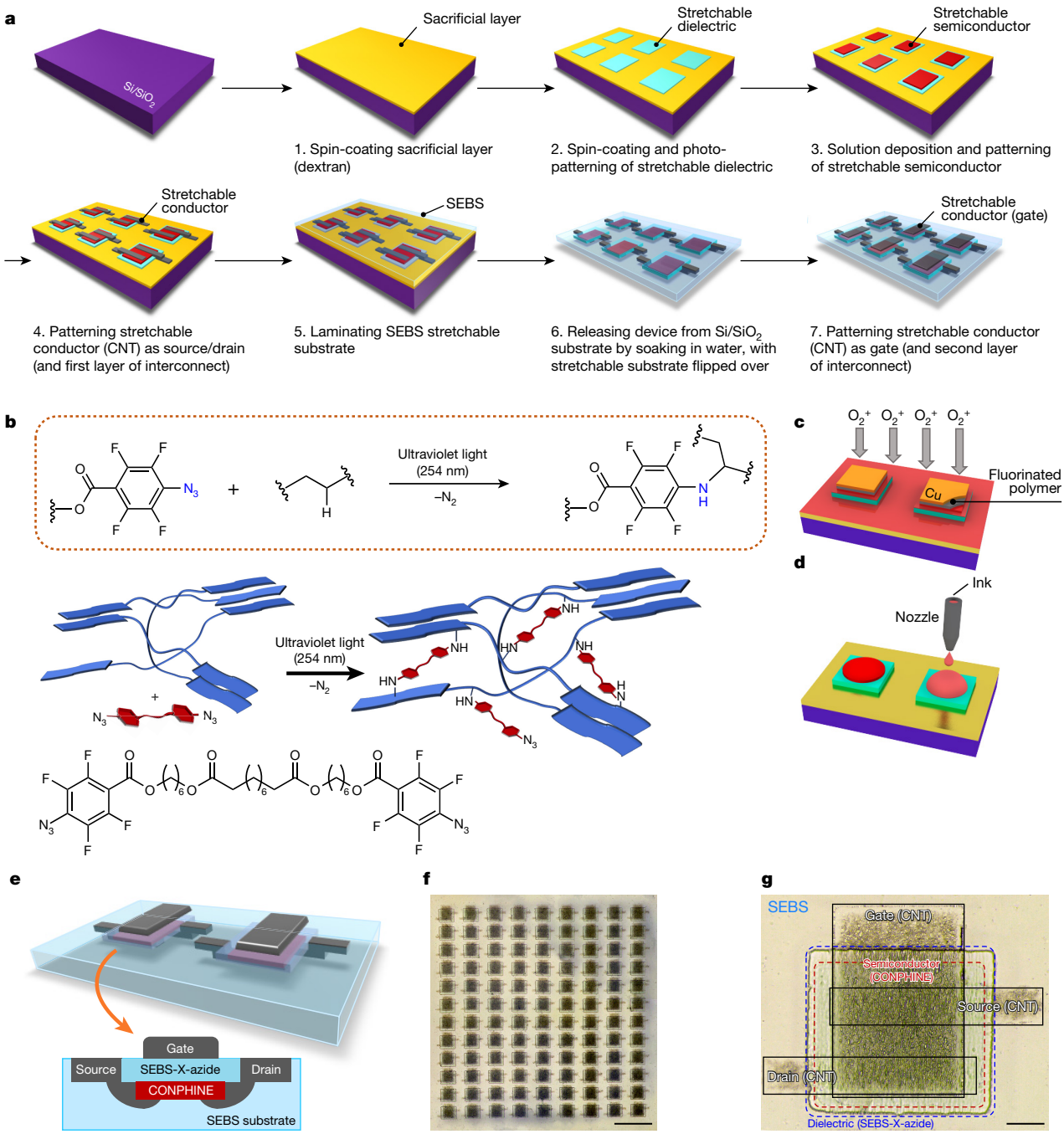


Figure 2 | Platform for fabricating intrinsically stretchable transistor arrays. a, Fabrication process flow. We begin with a Si/SiO_2 wafer that is coated with a water-soluble sacrificial layer (dextran). Next, a stretchable dielectric is deposited by spin coating and then photo-patterned (see panel **b**). A stretchable semiconductor is deposited by solution deposition and also patterned (see panels **c** and **d**). Stretchable conductors (carbon nanotubes, CNTs) are deposited and patterned as source and drain electrodes, together with the first layer of interconnect. A stretchable substrate (SEBS) is laminated on; soaking in water then releases the device from the rigid substrate. Finally, the gate electrodes (and the second layer of interconnect) are deposited and patterned to complete the transistor structure. **b**, Top, an azide-crosslinking reaction, which is initiated by ultraviolet light and is based on the reaction between azide groups and CH groups. Middle, how the polymer-chain network in an elastomer (blue, with rectangular planes representing rigid segments and tortuous lines representing soft segments) becomes crosslinked by azides (red) into a three-dimensional network. Bottom, chemical structure of an azide crosslinker. Azide crosslinking is a generally applicable strategy for photo-patterning intrinsically stretchable dielectrics. **c**, Etching-based process for patterning stretchable semiconductors. With the protection of patterned copper masks on top of a fluorinated polymer thin film (as the sacrificial layer), the stretchable semiconductor film is patterned by oxygen-plasma treatment. **d**, Inkjet printing as an additive patterning process for stretchable semiconductor film. **e**, Example of an intrinsically stretchable transistor array for performance characterization and demonstration. **f**, Optical microscopic image of a transistor array with 108 transistors. Scale bar, 1 mm. **g**, Magnified image of one transistor in the array. SEBS-X-azide, azide-crosslinked SEBS. Scale bar, 100 μm; channel length, 70 μm; channel width, 270 μm; gate dielectric thickness, 1.25 μm, capacitance, 1.75 nF cm^{-2}; semiconductor thickness, around 130 nm.

maximum 1.78 cm^2 V^{-1} s^{-1}) (Supplementary Fig. 12), showing the possibility of further improving the mobility by just improving the source/drain contacts. In addition, the power consumption of our intrinsically stretchable transistors, in the tens of microwatts, suggests the possibility of self-powered operations[29] for skin electronics.

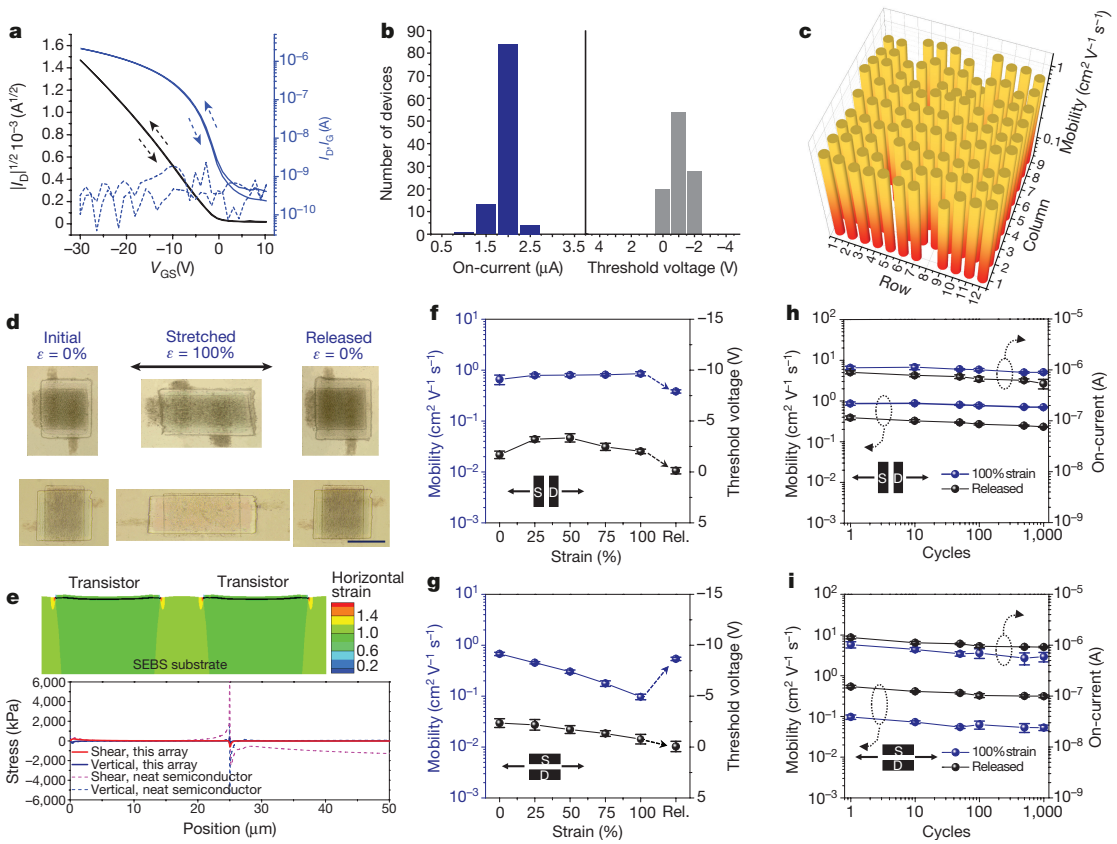


Figure 3 | Electrical performance and stretchability of the intrinsically stretchable transistor array. a, Typical transfer characteristics from the transistor array without strain showing little current hysteresis. I_D, drain current, represented by solid blue and black lines; I_G, gate current, represented by the dashed blue line; V_{GS}, the gate–source voltage. The applied drain–source voltage, V_{DS}, is −30 V. **b**, Histograms showing on-currents and threshold voltages from the 102 working transistors in the 108-transistor array. **c**, Map showing charge-carrier mobility for each transistor location. **d**, Optical microscope images showing the arrayed transistors stretched from 0% to 100% strain (ε) and then released, in directions both parallel (top) and perpendicular (bottom) to the channel. Scale bar, 250 μm. **e**, Top, mechanical simulations showing the strain distribution in the array when stretched to 100% strain (with the vertical dimension exaggerated by 25 times). Bottom, the shear stress and vertical stress distribution (under 40% global strain) at the dielectric layer's bottom interface ('this array'), and for a control structure in which the CONPHINE semiconductor layer was replaced with a neat conjugated polymer. 0 represents the dielectric edge and 25 μm represents the semiconductor edge. **f, g**, Mobilities and threshold voltages during a stretching cycle parallel (**f**) and perpendicular (**g**) to the channel direction. 'Rel.' refers to the values after releasing from 100% strain. S, source; D, drain. **h**, **i**, Mobilities and on-currents obtained under 100% strain and in a released state during 1,000 stretching cycles, parallel (**h**) and perpendicular (**i**) to the channel direction. The dashed circles and arrows point to the relevant *y*-axis. All data points in **f–i** represent average values obtained from five transistor devices for each set of stretching tests; error bars represent standard deviations.

Our transistor array can be stretched to 100% strain both parallel and perpendicular to the direction of charge transport, with no cracks, delamination or wrinkles observed (Fig. 3d). This is enabled by the 'quasi-homogeneous' mechanical structure design. With all of the major thin-film components being primarily SEBS based (that is, the dielectric, the substrate and 70% of the CONPHINE semiconductor), the interface shear and vertical stresses—the major causes of delamination under stretching—are effectively suppressed (Fig. 3e and Supplementary Fig. 13). The electrical performance of the transistors under channel-parallel stretching is highly stable even at 100% strain (Supplementary Fig. 14a, c), and even shows a slight increase in mobility to 0.99 $cm^2\ V^{-1}\ s^{-1}$ (Fig. 3f), probably owing to the strain-induced alignment of the conjugated polymer fibres in the CONPHINE film[16]. Upon releasing, the change in mobility possibly comes from the change in interface contact resulting from stretching-induced local plastic deformation, and also from the slight viscoelasticity of SEBS. Measured along the direction perpendicular to stretching, a highly stable transfer curve is maintained up to 100% strain (Supplementary Fig. 14b, d), while the slight decrease in mobility (Fig. 3g) agrees with reported characteristics for the CONPHINE film[16]. This intrinsically stretchable transistor array also shows unprecedented mechanical robustness when stretched repeatedly to 100% strain for 1,000 cycles in both directions (Fig. 3h, i and Supplementary Fig. 15). Furthermore, the array is exceptionally stretchable (up to 600% strain), and shows highly stable electrical performance even when subjected to pressure, twisting and biaxial stretching (Supplementary Fig. 16).

The high yield and performance uniformity of this fabrication platform has thus allowed us to develop intrinsically stretchable basic circuit elements (Fig. 1d)—the core of skin electronics. By incorporating scan and data interconnect lines, we achieved an intrinsically stretchable active matrix, with the same device density of 347 transistors per cm^2 (Fig. 4a). As a proof-of-concept demonstration of its application as the multiplexing backplane for skin electronics, we integrated this matrix with a 10 × 10 array of intrinsically stretchable resistive tactile sensors that are based on interdigitated carbon-nanotube electrodes (Fig. 4b and Extended Data Fig. 7), with a resolution of one sensor per 2 mm. The high stretchability allows the array to be attached conformably onto a human palm (with its naturally irregular surface and deformation) as a secondary skin (Fig. 4c and Supplementary Fig. 17), on which the location of a small artificial small ladybug with six conductive legs is accurately detected through a matched map of on-current magnitudes from the sensor pixels (Fig. 4d). This demonstrates the feasibility of using our intrinsically

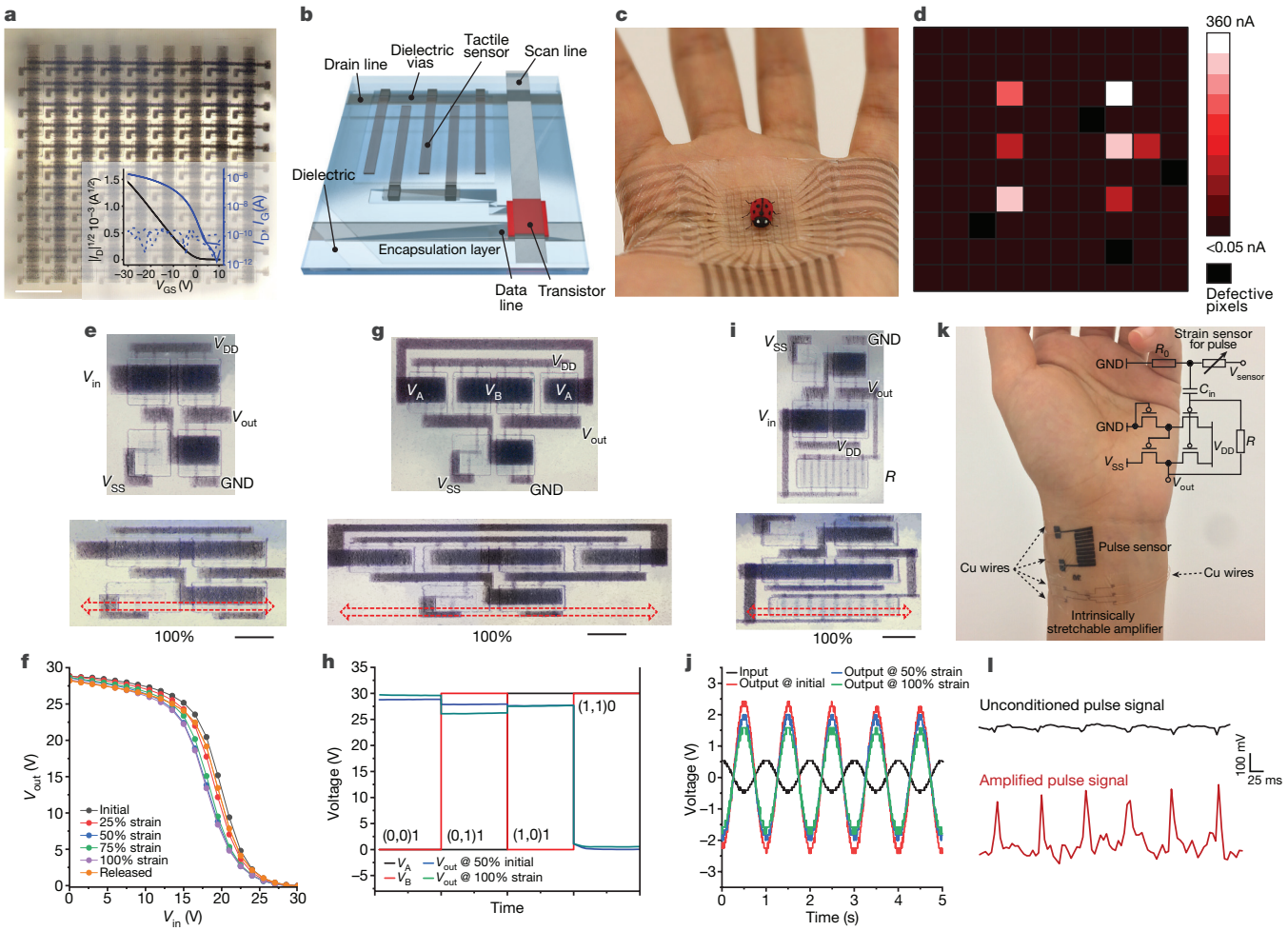


Figure 4 | Intrinsically stretchable circuits for skin electronics. **a**, A stretchable active matrix developed from our intrinsically stretchable transistor array. Scale bar, 1 mm. The inset shows a typical transfer curve recorded from a transistor in the matrix. **b**, Diagram showing a tactile sensor array made from a stretchable active matrix. **c**, The array adheres and conforms to a human palm, enabling accurate sensing of the position of a synthetic ladybug with six conductive legs. Voltages for the scan lines, data lines and drain lines are respectively −10 V, 0 and −10 V during the multiplexing measurement. ('Multiplexing' refers to a method by which one of multiple signals is selected and forwarded to a single channel at a time.) **d**, Current mapping in linear scale, showing exact matching with the position of the ladybug. **e**, Optical microscope images of a fabricated intrinsically stretchable inverter with pseudo-CMOS design, in its initial state (top) and after being stretched to 100% strain (bottom). **f**, Transfer curves from the inverter when stretched gradually from 0% to 100% strain. **g**, Optical microscope images of a fabricated intrinsically stretchable NAND gate in its initial state (top) and after being stretched to 100% strain (bottom). V_A and V_B are the input voltages at the A and B terminals. **h**, Output–input characteristics of the NAND gate at 0% and 100% strain. **i**, Optical microscope images of a fabricated intrinsically stretchable amplifier in its initial state (top) and after being stretched to 100% strain (bottom). **j**, Input sinusoidal signal, along with output signals after amplification when the amplifier is at 0%, 50% and 100% strain. **k**, Use of the intrinsically stretchable amplifier to amplify arterial pulse signals measured by a stretchable strain sensor. The devices are attached on skin side-by-side. Electrical connections are made using Cu wires (as marked), attached on the contacting pads by anisotropic conductive tapes. The inset shows the circuit diagram: R_0 is the divider resistor (680 kΩ); V_{sensor} is the direct-current voltage (40 V) applied to sensor and resistor; and C_{in} is the input capacitor (1 μF) for the amplifier. **l**, Pulse signals obtained, before and after amplification, using the same scale. In all of these circuits, the diode-type transistors have channels of length and width 80 μm; all the other transistors have channels of length and width 80 μm and 1,620 μm. GND, ground. For the electrical characterizations, the direct-current voltages applied to the electrodes indicated are $V_{DD} = 30$ V and $V_{SS} = -30$ V. All scale bars represent 600 μm.

stretchable active matrix as the backplane for high-resolution touch sensing in highly conformable electronic skins.

We also realized intrinsically stretchable circuits for signal manipulation and computation, which require higher complexity in terms of transistor interconnection and collective operation. We built basic building-block circuits for digital electronics using this transistor array. For example, an inverter based on a pseudo-CMOS design[30] (Fig. 4e and Extended Data Fig. 8a) gives the expected transfer behaviour, with the same range of input and output voltages, and little circuit-level bias-stress or electrical heating despite continuous operation (Supplementary Fig. 18). When gradually stretched to 100% strain, there is only a small shift in the transfer curve, which is acceptable for logic operations (Fig. 4f). We also built a NAND gate consisting of six transistors (Fig. 4g and Extended Data Fig. 8b), as a 'universal' logic gate for constructing all other logic gates. This shows stable logic operation even under 100% strain (Fig. 4h). For analogue circuits that interface directly with sensors, the basic component is an amplifier circuit. We successfully fabricated such an amplifier using a self-feedback design[31], with a non-gated transistor as the resistor (with resistance of the order of 10^8 Ω; Fig. 4i and Extended Data Fig. 8c); the signal amplification is maintained even at 100% strain (Fig. 4j and Supplementary Fig. 19). Next, to demonstrate skin electronics that contain both sensors and signal-processing units[32], we combined the amplifier with a stretchable pulse sensor[33] (Fig. 4k and Supplementary Fig. 20), achieving on-skin amplification of raw detected physiological signals (Fig. 4l). These basic circuit elements are now ready to be integrated into more

complex digital and analogue circuits, to realize more advanced signal-processing functionalities.

Compared with previously reported milestones in developing stretchable transistors and circuits for skin electronics (Extended Data Table 1), our intrinsically stretchable transistor array has, for the first time (to our knowledge), combined advanced electronic functionality with high skin-like stretchability. Moreover, our fabrication process provides a platform on which to readily incorporate future materials advancements into functional electronic circuits and systems with skin-like and even 'beyond-skin' softness and deformability.

Online Content Methods, along with any additional Extended Data display items and Source Data, are available in the online version of the paper; references unique to these sections appear only in the online paper.

Received 31 July; accepted 18 December 2017.
Published online 19 February 2018.

1. Gao, W. *et al.* Fully integrated wearable sensor arrays for multiplexed in situ perspiration analysis. *Nature* **529,** 509–514 (2016).
2. Kim, D. H. *et al.* Epidermal electronics. *Science* **333,** 838–843 (2011).
3. Son, D. *et al.* Multifunctional wearable devices for diagnosis and therapy of movement disorders. *Nat. Nanotechnol.* **9,** 397–404 (2014).
4. Tee, B. C. K. *et al.* A skin-inspired organic digital mechanoreceptor. *Science* **350,** 313–316 (2015).
5. Kang, S. K. *et al.* Bioresorbable silicon electronic sensors for the brain. *Nature* **530,** 71–76 (2016).
6. Minev, I. R. *et al.* Electronic dura mater for long-term multimodal neural interfaces. *Science* **347,** 159–163 (2015).
7. Khodagholy, D. *et al. In vivo* recordings of brain activity using organic transistors. *Nat. Commun.* **4,** 1575 (2013).
8. Li, S., Zhao, H. C. & Shepherd, R. F. Flexible and stretchable sensors for fluidic elastomer actuated soft robots. *MRS Bull.* **42,** 138–142 (2017).
9. Rus, D. & Tolley, M. T. Design, fabrication and control of soft robots. *Nature* **521,** 467–475 (2015).
10. Kaltenbrunner, M. *et al.* An ultra-lightweight design for imperceptible plastic electronics. *Nature* **499,** 458–463 (2013).
11. Matsuhisa, N. *et al.* Printable elastic conductors with a high conductivity for electronic textile applications. *Nat. Commun.* **6,** 7461 (2015).
12. Xu, S. *et al.* Soft microfluidic assemblies of sensors, circuits, and radios for the skin. *Science* **344,** 70–74 (2014).
13. Chortos, A. *et al.* Mechanically durable and highly stretchable transistors employing carbon nanotube semiconductor and electrodes. *Adv. Mater.* **28,** 4441–4448 (2016).
14. Chortos, A. *et al.* Highly stretchable transistors using a microcracked organic semiconductor. *Adv. Mater.* **26,** 4253–4259 (2014).
15. Liang, J. J. *et al.* Intrinsically stretchable and transparent thin-film transistors based on printable silver nanowires, carbon nanotubes and an elastomeric dielectric. *Nat. Commun.* **6,** 7647 (2015).
16. Xu, J. *et al.* Highly stretchable polymer semiconductor films through the nanoconfinement effect. *Science* **355,** 59–64 (2017).
17. Oh, J. Y. *et al.* Intrinsically stretchable and healable semiconducting polymer for organic transistors. *Nature* **539,** 411–415 (2016).
18. Scott, J. I. *et al.* Significantly increasing the ductility of high performance polymer semiconductors through polymer blending. *ACS Appl. Mater. Interfaces* **8,** 14037–14045 (2016).
19. Wang, Y. *et al.* A highly stretchable, transparent, and conductive polymer. *Sci. Adv.* **3,** e1602076 (2017).
20. Larson, C. *et al.* Highly stretchable electroluminescent skin for optical signaling and tactile sensing. *Science* **351,** 1071–1074 (2016).
21. Liang, J. J., Li, L., Niu, X. F., Yu, Z. B. & Pei, Q. B. Elastomeric polymer light-emitting devices and displays. *Nat. Photon.* **7,** 817–824 (2013).
22. Lipomi, D. J. *et al.* Skin-like pressure and strain sensors based on transparent elastic films of carbon nanotubes. *Nat. Nanotechnol.* **6,** 788–792 (2011).
23. You, I. *et al.* Stretchable E-skin apexcardiogram sensor. *Adv. Mater.* **28,** 6359–6364 (2016).
24. White, M. S. *et al.* Ultrathin, highly flexible and stretchable PLEDs. *Nat. Photon.* **7,** 811–816 (2013).
25. Png, R. Q. *et al.* High-performance polymer semiconducting heterostructure devices by nitrene-mediated photocrosslinking of alkyl side chains. *Nat. Mater.* **9,** 152–158 (2010).
26. Liu, L. H. & Yan, M. D. Perfluorophenyl azides: new applications in surface functionalization and nanomaterial synthesis. *Acc. Chem. Res.* **43,** 1434–1443 (2010).
27. Choi, W., Kim, M. H., Na, Y. J. & Lee, S. D. Complementary transfer-assisted patterning of high-resolution heterogeneous elements on plastic substrates for flexible electronics. *Org. Electron.* **11,** 2026–2031 (2010).
28. Singh, M., Haverinen, H. M., Dhagat, P. & Jabbour, G. E. Inkjet printing-process and its applications. *Adv. Mater.* **22,** 673–685 (2010).
29. Hwang, B. U. *et al.* Transparent stretchable self-powered patchable sensor platform with ultrasensitive recognition of human activities. *ACS Nano* **9,** 8801–8810 (2015).
30. Huang, T. C. *et al.* Pseudo-CMOS: a design style for low-cost and robust flexible electronics. *IEEE Trans. Electron Dev.* **58,** 141–150 (2011).
31. Sekitani, T. *et al.* Ultraflexible organic amplifier with biocompatible gel electrodes. *Nat. Commun.* **7,** 11425 (2016).
32. Koo, J. H. *et al.* Wearable electrocardiogram monitor using carbon nanotube electronics and color-tunable organic light-emitting diodes. *ACS Nano* **11,** 10032–10041 (2017).
33. Wu, Y. *et al.* High resolution flexible strain sensors for biological signal measurements. In *19th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers)* 1144–1147 (2017).

Supplementary Information is available in the online version of the paper.

Acknowledgements This work is supported by Samsung Electronics. We thank L. Beker, N. Matsuhisa and S. Chen for helping with experiments, and L. Jin for discussions about mechanical simulation. J.L. acknowledges support by the National Science Foundation Graduate Research Fellowship Program under grant DGE-114747. S.-K.K. thanks NETEP and MOTIE of the Republic of Korea (grant 20173010013000).

Author Contributions S.W., J.X. and Z.B. designed the project and experiments. S.W., J.X. and W.W. fabricated the intrinsically stretchable transistor array and circuits, and carried out electrical characterizations. G.-J.N.W. synthesized the azide compound. R.R. carried out mechanical simulations. S.W. and F.M.-L. undertook the inkjet printing of a semiconducting polymer. V.R.F. carried out X-ray photoelectron spectroscopy characterizations. J.W.C., A.M.F. and A.E. helped to prepare schematics for the three-dimensional transistor array and carried out device photography. J.X. and J.L. did the mechanical characterizations. S.-K.K. and A.G. provided conjugated polymers. T.L. helped with development of semiconductor patterning. S.N., Y.K., Y.Y. and B.M. helped with circuit design and measurements. S.W., Z.B., J.X. and J.B.-H.T. wrote the manuscript. All authors reviewed and commented on the manuscript.

Author Information Reprints and permissions information is available at www.nature.com/reprints. The authors declare no competing financial interests. Readers are welcome to comment on the online version of the paper. Publisher's note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations. Correspondence and requests for materials should be addressed to Z.B. (zbao@stanford.edu).

METHODS

Materials. All processing solvents, such as chlorobenzene, toluene, dodecane, hexane, 1,2,3,4-tetrahydronaphthalene (tetralin), 2-propanol, and ethoxynonafluorobutane, were purchased from commercial sources and used as received. The polymer semiconductor poly-[2,5-bis(7-decylnonadecyl)pyrrolo[3,4-c]pyrrole-1,4-(2H,5H)-dione-(E)-(1,2-bis(5-(thiophen-2-yl)selenophen-2-yl)ethene) (29-DPP-SVS) was synthesized as reported[34], as was poly(thiophen-2-yl)ethyl-2,5-bis(4-decyl tetradecyl)-2,5-dihydro-pyrrolo[3,4-c]pyrrole-1,4-dione-r-10%-2,6-pyridine-dicarboxamide (DPP2TTVT-PDCA)[17]. The number-averaged molecular weight and polydispersity of these polymers are shown in Supplementary Table 1. Number-average molecular weight (M_n), weight-average molecular weight (M_w), and polydispersity index (PDI) were evaluated by high-temperature size exclusion chromatography (SEC) using 1,2,4-trichlorobenzene and performed at 180 °C with an EcoSEC high-temperature gel permeation chromatography (GPC) device (Tosoh). This is equipped with a single TSKgel GPC column (GMH_{HR}-H; 300 mm × 7.8 mm), which was calibrated by monodisperse polystyrene standards. The azide crosslinker bis(6-((4-azido-2,3,5,6-tetrafluorobenzoyl)oxy)hexyl) decanedioate was synthesized as described below. The SEBS compounds H1221 and H1052, with poly(ethylene-co-butylene) volume fractions of respectively 88% and 80%, were provided by the Asahi Kasei company. SEBS rubbers have been reported to have good long-term stability and biocompatibility[35,36]. We use SEBS H1052 as a stretchable dielectric layer, and SEBS H1221 in the CONPHINE semiconductor and also as the stretchable substrate in the intrinsically stretchable transistor array. PU SG80A was supplied by Lubrizol. Dextran was purchased from Sigma-Aldrich and used as received. Carbon nanotubes for electrodes were purchased from Carbon Solutions (P3-SWNTs). Methyl pentafluorobenzoate and sebacoyl chloride were purchased from Oakwood Chemical and ACROS Organics, respectively, and used as received. Other commercial reactants were purchased from Sigma-Aldrich and used without further purification.

Fabrication of the intrinsically stretchable transistor array. As the substrate for the fabrication process, a Si/SiO_2 wafer was first cleaned with oxygen plasma (150 W, 200 mTorr) for 2 min, and then sonicated in acetone, 2-propanol and deionized water for 5 min each. After the wafer was blown dry with nitrogen gas, a dextran solution (10 wt% in water) was spin-coated on top at 1,500 r.p.m. for 20 s. The wafer was then baked on a hot plate at 80 °C for 1 min and 180 °C for 30 min to fully remove the trapped water in the film. Then, a solution containing SEBS (H1052) with azide crosslinker (60 mg ml^{-1} for SEBS and 2.4 mg ml^{-1} for azide in toluene) was spin-coated on top at 1,000 r.p.m., to form a stretchable dielectric film with a thickness of about 1.25 μm. Subsequently, the SEBS–azide film was photo-patterned by exposure under deep ultraviolet light (wavelength 254 nm, using a Spectrum 100 Precision UV Spot Curing System from American Ultraviolet) for 4 min with a dose of about 540 mJ cm^{-2}, to initiate the photo-crosslinking reaction in selective areas defined by a mask. Soft baking was carried out at 120 °C for 15 min in air on a hot plate to further increase the degree of crosslinking in photo-exposed areas. After this, dodecane was used to dissolve the unexposed areas of SEBS, with the exposed areas preserved. In order to fully crosslink these preserved areas, the device was further baked at 200 °C for 1 h in a glovebox.

The surface of the patterned SEBS ('SEBS-X-azide') dielectric was modified by octadecyltrimethoxysilane (OTS) molecules to increase the hydrophobicity, through consecutive processes of O_2 plasma treatment, spin-coating of OTS solution (3 mM in hexane) at 3,000 r.p.m., and finally vapour annealing in a desiccator with a small vial containing a few millimetres of ammonium hydroxide solution (28–30% in water) for 10 h at room temperature. Then, the CONPHINE semiconductor film was deposited on top by spin-coating of 29-DPP-SVS-(1)/SEBS-H1221 solution (10 mg ml^{-1} in chlorobenzene, with a weight ratio of 3:7) at 1,000 r.p.m., followed by annealing at 150 °C on a hotplate in a glovebox. A fluorinated polymer solution (3M Novec 1902 Electronic Grade Coating diluted by ethoxynonafluorobutane in a 1/2 volume ratio) was spin-coated at 1,000 r.p.m. to give the fluorinated sacrificial layer. Copper patterns (200 nm) as etching masks were deposited on top by thermal evaporation, through a shadow mask aligned with the stretchable dielectric pattern. Etching of the CONPHINE semiconductor film in the areas uncovered by the patterned copper films was performed in O_2 plasma (150 W, 200 mTorr). Then, the copper films were lifted off by soaking the device in ethoxynonafluorobutane to dissolve the fluorinated polymer sacrificial layer, only leaving the CONPHINE semiconductor patterns on top of the SEBS dielectric patterns. Top source/drain electrodes were patterned by spray-coating carbon nanotube (CNT) solution through a shadow mask (Invar). The CNT solution is prepared by dispersing 20 mg P3-SWNT in 70 ml 2-propanol with two drops of water, through consecutive 3-h bath sonication, 10-min tip sonication and then centrifugation. In order to improve the resolution of the spray-coated CNT electrodes, we placed a piece of magnet underneath the sample to hold the shadow mask tightly to the sample, and optimized the spray-coating condition to the sample temperature of about 75 °C, the flow rate of 2.8 ml min^{-1}, and the gun-to-sample distance of about 12 cm.

In the next fabrication step, a SEBS (H1221) stretchable substrate was conformably laminated onto the fabricated array devices on the Si substrate. Then, the array was transferred onto the stretchable substrate by immersing the entire device in water to dissolve the sacrificial dextran layer. Finally, the gate electrodes were patterned on top of the SEBS dielectric by spray-coating the above-described CNT solution through a shadow mask. The fabricated intrinsically stretchable transistor array was baked at 80 °C under vacuum for 4 h to fully remove the moisture, before electrical characterization. Alignment of the shadow masks was performed under optical microscopy.

Photo-patterning of polyurethane using azide crosslinking. A polyurethane (SG80A) solution with azide crosslinker (40 mg ml^{-1} polyurethane; 1.6 mg ml^{-1} azide in tetrahydrofuran) was spin-coated at 1,000 r.p.m. onto a Si substrate, to form a stretchable dielectric film with a thickness of about 1.2 μm. The polyurethane–azide film was then photo-patterned by exposure under deep ultraviolet light (wavelength 254 nm) for 9 min with a dose of around 1,215 mJ cm^{-2}, to initiate the photo-crosslinking reaction in selective areas defined by the mask. The film was then soft baked at 120 °C for 15 min in air, and developed in *n*-methyl-2-pyrrolidon (NMP), before further baking at 200 °C for 1 h in a glovebox.

Surface modification of patterned SEBS dielectric. The morphology of a CONPHINE film obtained by spin-coating of the solution depends strongly on the surface energy of the substrate. When CONPHINE film is spin-coated on crosslinked SEBS, the SEBS phase in the CONPHINE film is strongly attracted by the dielectric surface, expelling almost all of the conjugated polymers to the top surface of the film (as shown by X-ray photoelectron spectroscopy (XPS) in Extended Data Fig. 6e). The strong mutual interaction in the conjugated polymer phase leads to the formation of a dense network with many large aggregates and junctions (Extended Data Fig. 6b). This morphology might create excess boundaries for charge transport at the aggregates and junctions, and leads to a relatively low charge mobility of 0.31 $cm^2 V^{-1} s^{-1}$ (Extended Data Fig. 6g). In order to turn this morphology into the nanoscale-confined fibre network that favours efficient charge transport, we modify the crosslinked SEBS surface with OTS molecules to increase the hydrophobicity and thereby reduce the attraction to the SEBS phase in the CONPHINE film. Through such surface modification, the water contact angle of crosslinked SEBS increases from 94° to 102° (Extended Data Fig. 6a, b), indicating decreased surface energy. The CONPHINE film spin-coated on this OTS-modified crosslinked SEBS now produces a morphology with a gradually reduced distribution of the conjugated polymer phase throughout the CONPHINE film from the top surface to the bottom surface. The conjugated polymer phase at the top surface forms the ideal nanoconfined morphology without observable large aggregates (Extended Data Fig. 6d). The charge-carrier mobility thereby increases to 0.76 $cm^2 V^{-1} s^{-1}$ (Extended Data Fig. 6h).

Inkjet printing of polymer semiconductor. Inkjet printing was done using a Dimatix Materials printer (DMP-2850). The polymer semiconductor 29-DPP-SVS-(*2*) (M_n = 30.1 kDa) was dissolved in tetralin, producing a concentration of 3 mg ml^{-1}. After filtering, the solution was filled into the printing cartridge, and then desiccated for 20 min. During printing onto SEBS dielectric patterns, the drop-to-drop distance was set to 30 μm, with two adjacent nozzles used at the same time. The temperature of the sample platen was set to 40 °C. The polymer semiconductor patterns aligned on SEBS patterns were obtained using five layers of consecutive printing in order to get enough polymer materials deposited for good performance. Annealing at 150 °C for 30 min in a glovebox, and for another 30 min in a vacuum, led to better crystallization and full removal of the solvent. To evaluate performance, gold was deposited through the aligned shadow mask, as the top contact source/drain electrodes for constructing thin-film transistor structures.

The stretchability of the 29-DPP-SVS-(2) patterns obtained by inkjet printing was compared with that of the 29-DPP-SVS-(2) spin-coated films patterned by copper-protected etching. For both processes, the 29-DPP-SVS-(2) semiconductor was patterned on top of azide-X-SEBS film on dextran-coated Si/SiO_2 substrate. Then, the 29-DPP-SVS-(2) patterns together with the SEBS dielectrics were transferred to polydimethylsiloxane (PDMS) stamps by dissolving the dextran layer in water. After stretching to 100% strain, the 29-DPP-SVS-(2) patterns on the azide-X-SEBS dielectric film were transferred to a Si/SiO_2 substrate. Finally, gold electrodes were evaporated on top to allow mobility measurements. Initial mobilities were also obtained after the same transferring process to Si/SiO_2 substrates in order to maintain comparative experimental conditions.

Fabrication of an active-matrix tactile sensor array. The active-matrix part was fabricated in a similar way to the intrinsically stretchable transistor array, with the same fabrication conditions for all corresponding material components. A Si/SiO_2 wafer was used as the substrate, with dextran solution (10 wt% in water) spin-coated as the sacrificial layer at 1,500 r.p.m for 20 s. It was dried by baking at 80 °C for 1 min, and then baked at 180 °C for 30 min to fully remove any trapped

water. Next, a thin film of SEBS was photo-patterned through azide-crosslinking chemistry, forming the dielectric layer with via-openings that allow the electrical connection between transistor and tactile sensor. A CONPHINE film as the semiconductor layer was spin-coated on top and patterned by the etching-based strategy described earlier. Carbon nanotubes were then spray-coated through a shadow mask to form stretchable data lines, source and drain electrodes for the transistors, and drain lines (Fig. 4b). A thin layer of SEBS substrate was laminated on top for transferring the device; soaking in water then dissolved the dextran sacrificial layer. On the reverse of the device, scan lines (as gate electrodes for the transistor) and interdigitated electrodes for the tactile sensors were fabricated by spray-coating of carbon nanotubes through a shadow mask.

An encapsulation layer that exposes just the tactile sensor elements was fabricated by photo-patterning a SEBS thin film (spin-coated from a solution of 80 mg ml^{-1} SEBS and 3.2 mg ml^{-1} azide in toluene) through azide-crosslinking chemistry, on top of a dextran-coated Si/SiO_2 substrate. The active-matrix tactile sensor array described above, supported by a glass slide, was laminated onto this encapsulation layer, with alignment achieved under an optical microscope. Finally, the entire device was released from the Si/SiO_2 substrate by soaking in water to dissolve the dextran. Baking at 80 °C under a vacuum for 4 h fully removed any moisture before electrical characterization.

Fabrication of a resistive strain sensor for pulse monitoring. A 50-μm-thick commercial polyimide tape was attached to a silicon wafer that served as a large, flat, and heat-conductive substrate. Laser-induced porous graphite structures were patterned by direct writing with a CO_2 laser on the polyimide film, as described[33]. The SEBS/toluene solution was poured onto the patterned sample, and the solvent allowed to evaporate gradually. After the SEBS film (thickness 0.1 mm) had solidified fully, the graphite strain sensor could be peeled off by hand from the polyimide tape and transferred onto the SEBS film. Finally, to protect the porous graphite pattern from peeling off when making contact with an object, the whole structure was sealed with another thin PDMS layer of about 0.05 mm in thickness.

Material and device characterizations. Mechanical strain–stress and cyclic stress–strain experiments of crosslinked and uncrosslinked SEBS films were performed using an Instron 5565 instrument. Creep recovery was tested through dynamic mechanical analysis (using a TA Instrument Q800 with tension clamps). Crosslinked SEBS films were spin-coated from 150 mg ml^{-1} toluene solution at a speed of 300 r.p.m. for 3 min. The spin-coated films were then laminated several times to form a thick film (about 0.05 mm thick) for clamping. The thick film was further crosslinked at 200 °C for 1 h in a glovebox. An SEBS sample film was prepared in the same way. These films were then used for strain–stress and creep-recovery experiments.

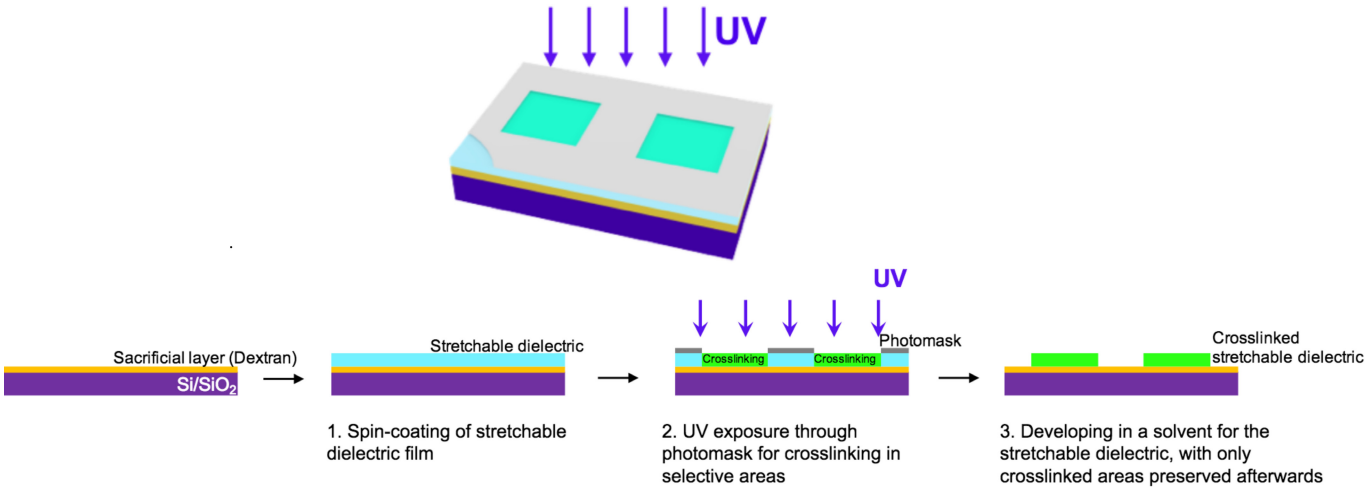
X-ray photoelectron spectroscopy (XPS) characterization was performed using a PHI VersaProbe III scanning XPS microprobe. For depth profiling, sputtering was carried out using an argon 2500+ gas cluster ion beam gun at 5 kV and 15 mA, with 1 min of sputtering per cycle. An SEBS film of known thickness was used to calibrate the sputtering rate, which was 3 nm min^{-1}. The dielectric constants of SEBS before and after azide crosslinking were obtained through capacitance measurement with an Agilent precision LCR meter E4980A. Nuclear magnetic resonance (NMR) spectra were recorded on a Varian Mercury console spectrometer (^{1}H 400 MHz, ^{19}F 400 MHz, ^{13}C 100 MHz). Chemical shifts are given in parts per million (p.p.m.) with respect to tetramethysilane as an internal standard, and coupling constants (J) are given in hertz (Hz).

All of the electrical characteristics of the transistors were measured using a probe station in an ambient environment connected to a Keithley 4200 characterization system. Characterizations of the circuits were also performed using the probe station. The inverter and the NAND circuits were characterized using the Keithley 4200 coupled to an extra direct-current power supply. The amplifier circuit was characterized using a functional generator (Velleman PCSGU250) to generate the sinusoidal input signal and an oscilloscope (Velleman PCSGU250) with a 10/1 probe to measure the output signal, with a AC-coupling capacitor (2μF) added at both input and output ends. The active-matrix tactile sensor array on a human palm was electrically connected to external copper wires using anisotropic conductive tapes. Static tactile mapping of the artificial ladybug was performed with the Keithley 4200 using a manual switch.

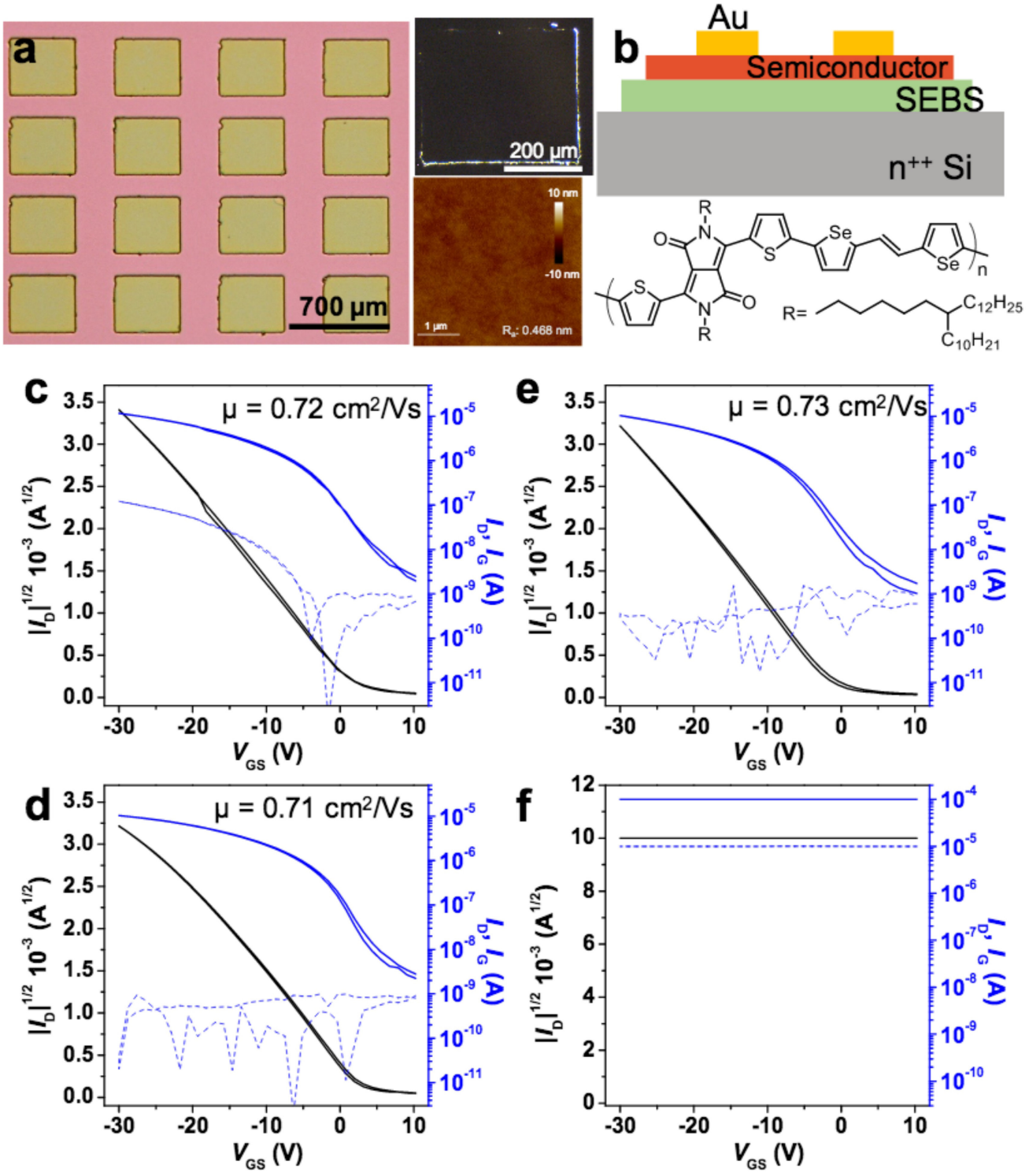
Testing the devices on human hands. The tests of devices on human hands described herein do not need Institutional Review Board (IRB) approval, because our experiments do not affect living people physically or physiologically, and we have not sought or received identifiable private information. The hands shown in Figs 1, 4 and Supplementary Figs 17, 20 are those of J. Xu and S. Wang, who have given their consent to publish these images.

Data availability. The data that support the findings of this study are available from the corresponding author on reasonable request.

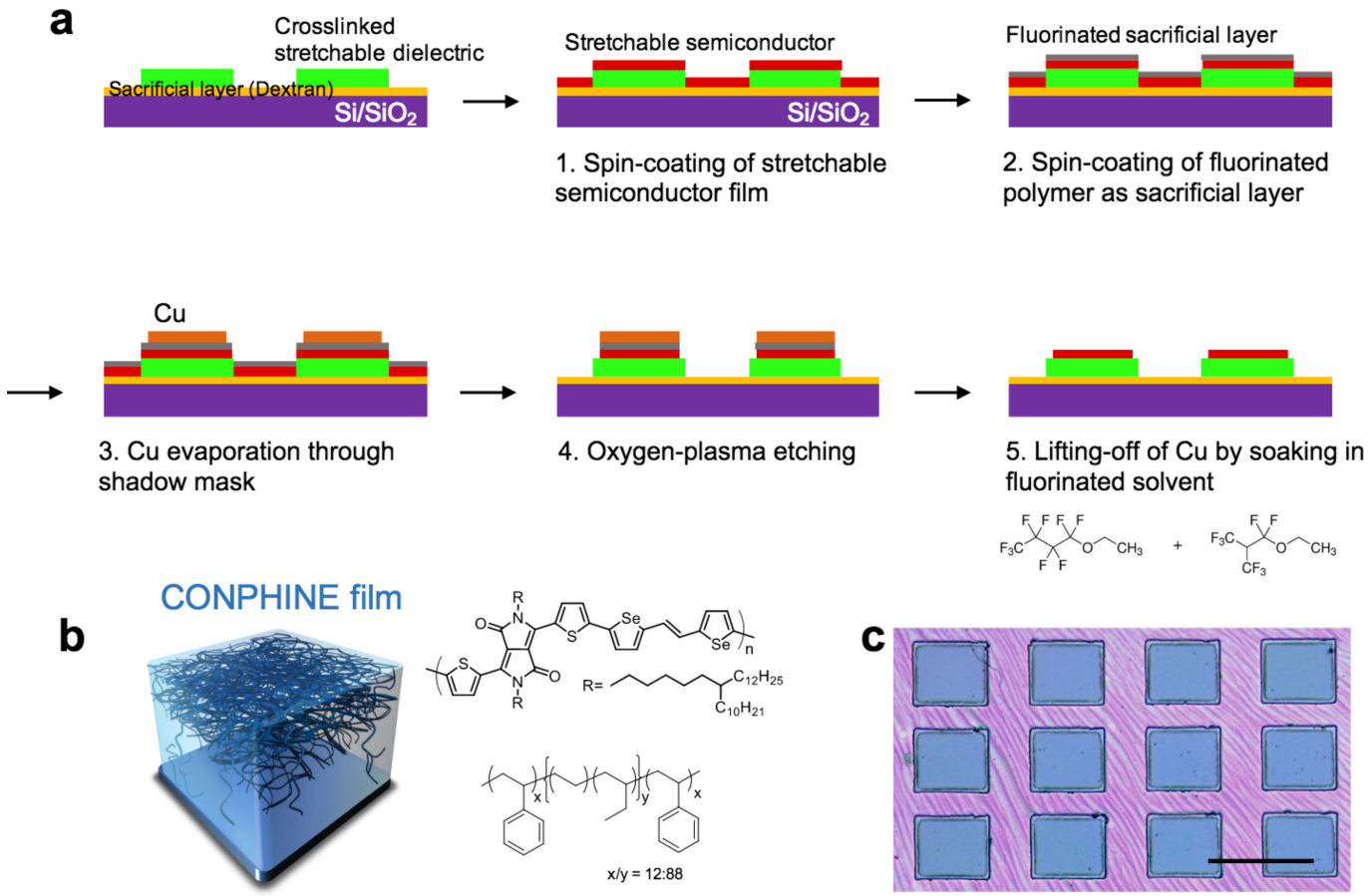
34. Kang, I., Yun, H. J., Chung, D. S., Kwon, S. K. & Kim, Y. H. Record high hole mobility in polymer semiconductors via side-chain engineering. *J. Am. Chem. Soc.* **135,** 14896–14899 (2013).
35. Guillemette, M. D., Roy, E., Auger, F. A. & Veres, T. Rapid isothermal substrate microfabrication of a biocompatible thermoplastic elastomer for cellular contact guidance. *Acta Biomater.* **7,** 2492–2498 (2011).
36. Borysiak, M. D. *et al.* Simple replica micromolding of biocompatible styrenic elastomers. *Lab Chip* **13,** 2773–2784 (2013).
37. Kim, D.-H. *et al.* Stretchable and foldable silicon integrated circuits. *Science* **320,** 507–511 (2008).
38. Sekitani, T. *et al.* A rubberlike stretchable active matrix using elastic conductors. *Science* **321,** 1468–1472 (2008).
39. Cai, L., Zhang, S., Miao, J., Yu, Z. & Wang, C. Fully printed stretchable thin-film transistors and integrated logic circuits. *ACS Nano* **10,** 11459–11468 (2016).



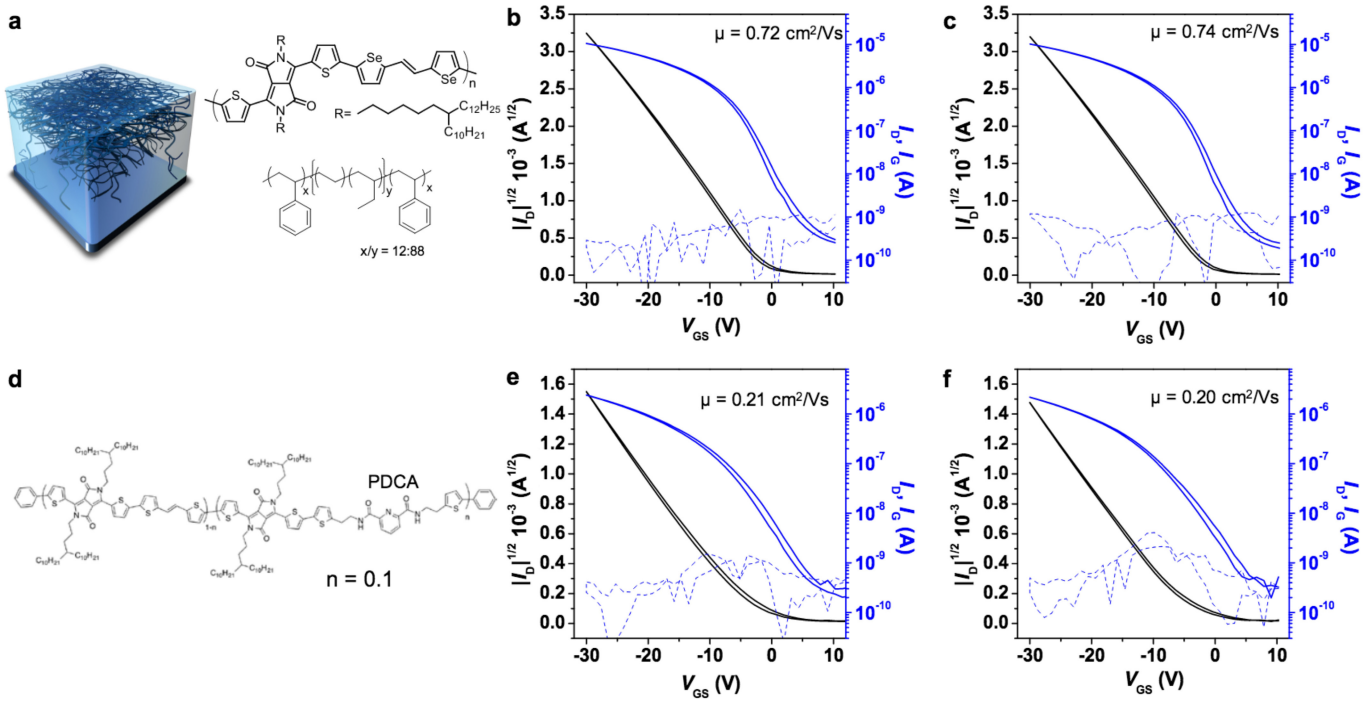
Extended Data Figure 1 | A direct photo-patterning process for fabricating stretchable dielectrics. Top, diagram of the stretchable dielectric undergoing ultraviolet-triggered azide crosslinking through a mask (grey). Bottom, detailed steps of the process.



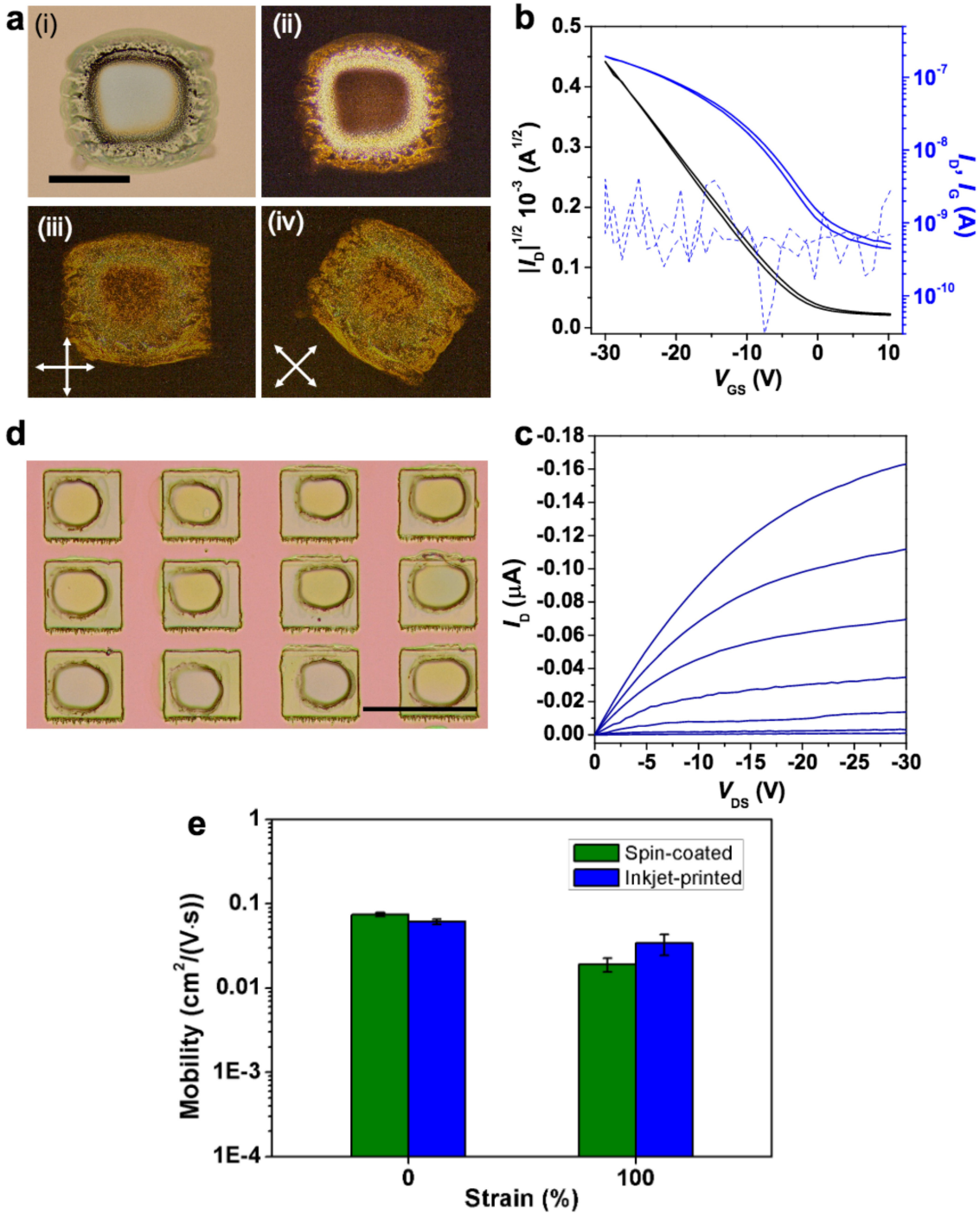
Extended Data Figure 2 | A photo-patterned SEBS film constitutes a solvent-resistant, stretchable dielectric layer for organic thin-film transistors. a, Optical microscope images (left, bright field; top right, dark field) of a photo-patterned SEBS film. Bottom right, an image of the surface taken using an atomic-force microscope (AFM), showing the very small roughness value ($R_a = 0.468$ nm) produced after patterning. **b**, Top, diagram showing an azide-crosslinked SEBS film with semiconductor on top, constituting an organic field-effect transistor. Bottom, chemical structure of the semiconductor layer in the diagram above. We made these transistors to test the solvent resistance of the azide-patterned SEBS film, to ensure that it could allow direct spin-coating of semiconductor solution (with chlorobenzene as the solvent) on top. Channel length, 50 μm; channel width, 1,000 μm; gate dielectric capacitance, 1.75 nF cm^{-2}. **c**, Transfer curve of a transistor that was obtained by transferring semiconductor film onto azide-patterned SEBS. In this case, the semiconductor film was obtained by spin-coating its solution onto an OTS-treated SiO_2 surface.**d**, Transfer curve for a transistor that was obtained by directly spin-coating the semiconductor onto azide-patterned SEBS. The similar mobility (μ) in **c** and **d** indicates that the semiconductor can be spin-coated directly onto the solvent-resistant, azide-patterned SEBS. **e**, Transfer curve for a transistor with the semiconductor film transferred onto unpatterned (uncrosslinked) SEBS. This semiconductor film was obtained by spin-coating its solution onto an OTS-treated SiO_2 surface. The similar mobility in **c** and **e** indicates that azide crosslinking does not change the ability of SEBS to function as a dielectric. **f**, Transfer curve for a transistor with the semiconductor film directly spin-coated onto unpatterned (uncrosslinked) SEBS, during which the SEBS dielectric is completely destroyed by the solvent.



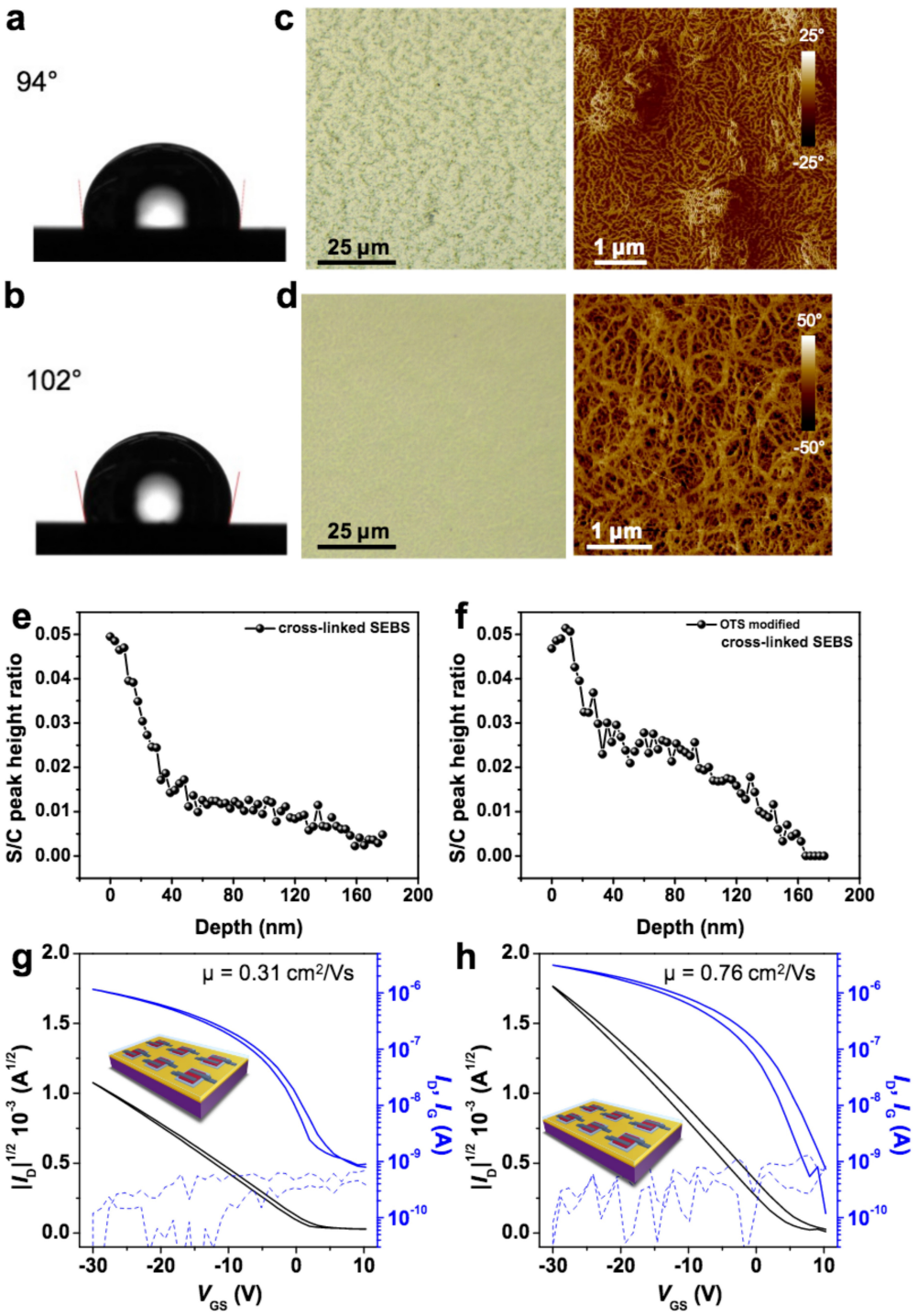
Extended Data Figure 3 | Etching-based patterning for stretchable semiconductors. a, Detailed patterning steps. **b**, Diagram of the CONPHINE semiconducting film, which is composed of 70 wt% SEBS (x/y = 12:88) and 30 wt% semiconductor phase, with both chemical structures shown on the right. **c**, Optical microscopic image of the patterned CONPHINE film aligned on top of SEBS patterns; scale bar, 700 μm.



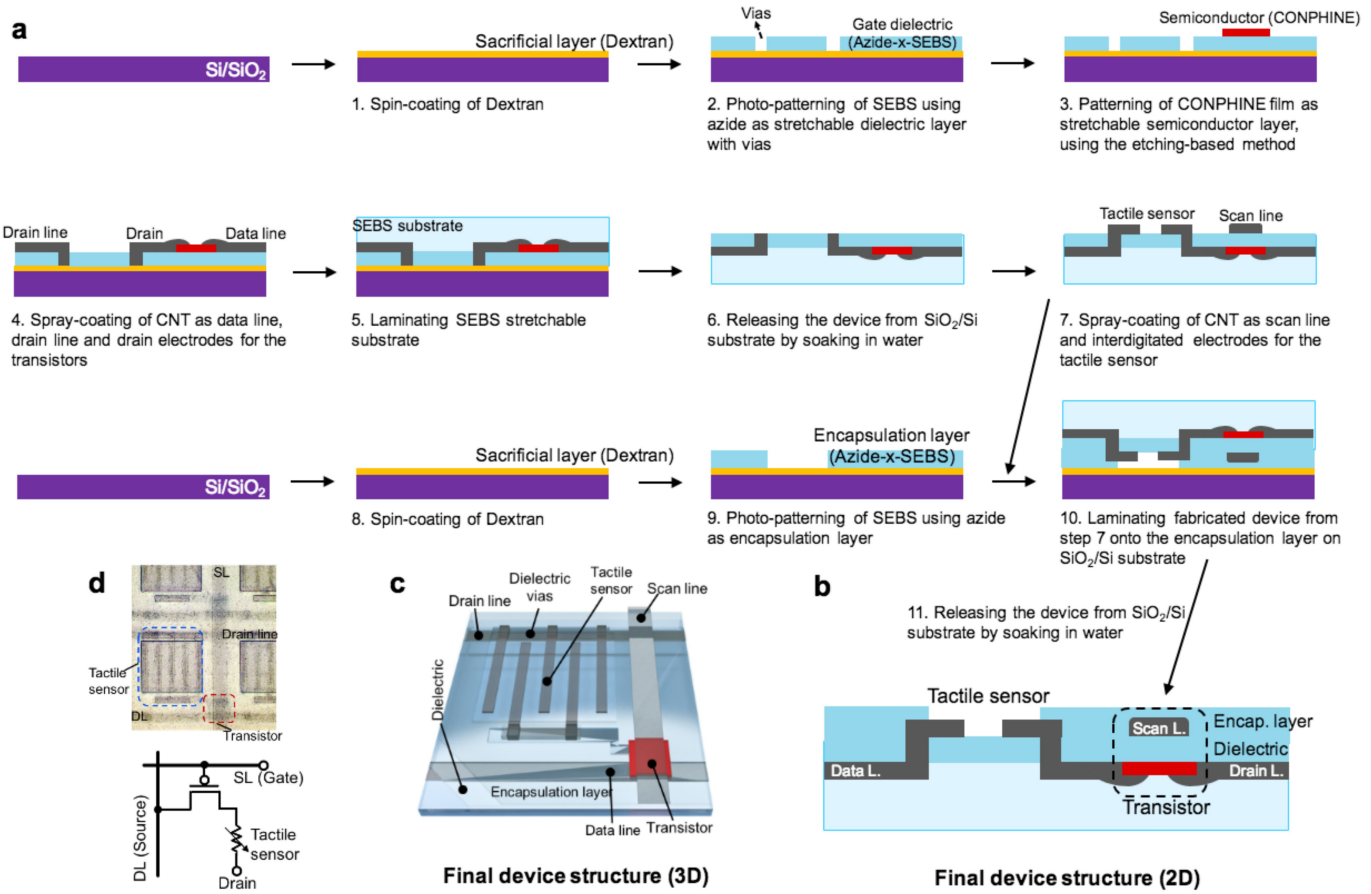
Extended Data Figure 4 | Test of the etching-based patterning method on different stretchable semiconductors. a, CONPHINE film. **b**, **c**, Its electrical performance in a thin-film transistor before (**b**) and after (**c**) patterning. **d**, A conjugated polymer (DPP2TTVT-PDCA) with hydrogen bonding that is built from 2,6-pyridine dicarboxamide (PDCA) moieties. **e, f**, Its electrical performance in in a thin-film transistor before (**e**) and after (**f**) patterning. All the thin-film transistors for testing have the device structure shown in Extended Data Fig. 2b.



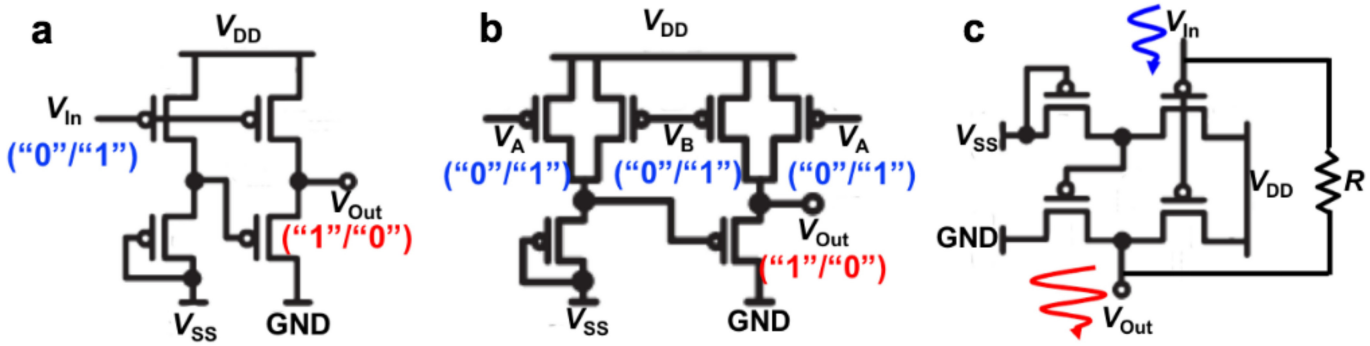
Extended Data Figure 5 | Inkjet-printed polymer semiconductor pattern on an azide-crosslinked SEBS dielectric. a, Optical microscope images of a typical printed pattern of 29-DPP-SVS-(2). **i**, Bright field. **ii**, Dark field. **iii**, **iv**, Cross-polarized images. **b**, Transfer characteristics of a transistor made from such an inkjet-printed semiconductor pattern, with thermally evaporated gold for the top contact electrodes. The transistor gives ideal transfer behaviour with no hysteresis. The obtained average mobility is 0.072 cm^2 V^{-1} s^{-1}. **c**, Corresponding output curve for this transistor. Here, even though its drop-casting-like deposition and crystallization of the semiconductor polymer may not give the best electrical performance (or, possibly, stretchability), the inkjet printing process is convenient as it involves fewer steps. **d**, Optical microscopic image of printed 29-DPP-SVS-(2) patterns aligned on top of SEBS patterns. Scale bar, 700 μm. **e**, Initial mobility and stretchability (the latter reflected by mobility at 100% strain along the charge-transport direction) of 29-DPP-SVS-(2) patterns obtained by inkjet printing, compared with patterns obtained by spin-coating with copper-protected etching. Inkjet printing gives slightly lower initial mobility than spin-coating, but slightly better stretchability.



Extended Data Figure 6 | Morphology and performance optimization of a CONPHINE film directly spin-coated on an azide-crosslinked SEBS surface, through surface modification with OTS. a, b, Contact angles of water on unmodified azide-crosslinked SEBS (**a**) and OTS-modified azide-crosslinked SEBS (**b**). **c, d**, Surface morphology (left, optical microscopic images; right, AFM images) of CONPHINE film on unmodified azide-crosslinked SEBS (**c**) and OTS-modified azide-crosslinked SEBS (**d**). **e**, **f**, XPS characterization of sulfur/carbon peak height ratios, showing the vertical distribution of the semiconductor phase in CONPHINE films obtained on unmodified azide-crosslinked SEBS (**e**) and on OTS-modified azide-crosslinked SEBS (**f**). Given that sulfur appears only in conjugated polymers, the ratio of the sulfur 2*p* to carbon 1*s* peaks qualitatively reflects the amount of conjugated polymer at different depths. **g**, **h**, Performance of transistor arrays fabricated on Si/SiO_2 substrates with CNTs as source/drain electrodes, spin-coated CONPHINE film as the semiconductor layer, and unmodified azide-crosslinked SEBS (**g**) or OTS-modified azide-crosslinked SEBS (**h**) as the dielectric layer.



Extended Data Figure 7 | Fabrication and structure of an intrinsically stretchable, active-matrix tactile sensor array. a, Fabrication steps. **b**, Two-dimensional device structure. **c**, Three-dimensional device structure. **d**, Optical microscope image and circuit diagram of one pixel in the stretchable active-matrix tactile sensor array, showing the connection between the transistor and the corresponding tactile sensor. With the tactile sensors connected between the drain lines and the transistor drain electrodes through the dielectric's via holes, their resistance change from contact with conductive objects (including human skin) can be sampled by the drain currents through the transistors.



Extended Data Figure 8 | Circuit diagrams of the intrinsically stretchable circuits. a, Inverter. **b**, NAND. **c**, Amplifier.

Extended Data Table 1 | Comparison of our intrinsically stretchable transistor array with previous milestone works on stretchable transistors

		Buckling method		Rigid-island with stretchable interconnect		Intrinsically stretchable					
Ref.	**This work**	10	37	38	11	15	17	16	13	14	39
Semiconductor	29-DPP-SVS /SEBS (*polymer*)	DNTT (*organic small molecule*)	Si	Pentacene (*organic small molecule*)	DNTT (*organic small molecule*)	CNT	DPP2TTVT-PDCA (*polymer*)	DPPT-TT/SEBS (*polymer*)	CNT	P3HT (*polymer*)	CNT
Dielectric	SEBS	AlO_x/SAM	SiO_2	Polyimide	AlO_x/SAM	PU	PDMS	SEBS	PU	PU	$BaTiO_3$/PDMS
Conductor	CNT	Au	Cr/Au	Ag nanoparticles	Au	CNT	CNT	CNT	CNT	CNT, liquid metal	CNT
Mobility ($cm^2/(V{\cdot}s)$)	1.37 (ave.) 1.78 (max.)	0.88 (ave.)	290 (n-type) 140 (p-type)	c.a. 0.48 (ave.)	1.8 for single transistor	27.0 (ave.) 32.5 (max.)	0.28 (ave.) 0.6 (max)	0.59 (ave)	0.18 (ave.)	0.034	~4
Density (cm^{-2})	347	c.a. 5	c.a. 280	*Not reported*	c.a. 4	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*	c.a. 4 (4 devices)
Driving voltage (V)	10-30	5	5	100	3	8	60	40	60	80	30
On-current (μA/mm)	7.4	120	c.a. 1300	0.42	3.3	52	2.8	2.5	5	c.a. 0.73	14.4
Demonstrated stretchability	600% strain for 1 cycle; 100% strain for 1000 cycles	100% strain for 200 cycles (*single device*)	5% strain without cycling	70% strain without cycling	110% strain for 1 cycle (4 devices, density of ~0.4 cm^{-2})	50% strain for 1 cycle; 20% strain for 500 cycles	100% strain for 1 cycle; 25% strain for 500 cycles	100% strain for 1 cycle; 25% strain for 1000 cycles	100% strain for 1000 cycles	40% for 100 cycles	50% strain for 1400 cycles
Integrated functionality	Active matrix, digital and analog circuits	Active matrix (non-stretchable)	Digital and analog circuits	Active matrix	Active matrix (2 × 2)	*N/A*	*N/A*	*N/A*	*N/A*	*N/A*	Digital circuits (with non-ideal performance)

We compare data on our transistor array with data on previous milestone approaches to skin electronics[10,11,13–17,37–39], in terms of the materials used, key parameters on electrical performance, and skin conformability (represented by stretchability).