SPATIALLY RESOLVED ELECTRICAL TRANSPORT IN CARBON-BASED NANOMATERIALS

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Nanoscale materials based on the element carbon have attracted tremendous attention over the years from a diverse array of scientific disciplines. There is particular interest in the development of such materials for electronic device applications, thus requiring comprehensive studies of their electrical transport properties. However, in systems with reduced dimensionality, the electrical behavior may show significant variation depending on the local physical structure. Therefore, it would be most ideal to understand these two facets simultaneously. In this thesis, we study electrical transport in carbon nanotubes, pentacene thin films, and graphene in a spatially resolved manner in combination with two different microscopy techniques. With photoelectrical microscopy, we first image the electrical conductance and transport barriers for individual carbon nanotubes. We then resolve the precise points where charge injection takes place in pentacene thin-film transistors and explicitly determine the resistance for each point contact using the same technique. Finally, we study the polycrystalline structure of large-area graphene films with transmission electron microscopy and measure the electrical properties of individual grain boundaries.

BIOGRAPHICAL SKETCH

Wei grew up in Palo Alto, California and attended Henry M. Gunn High School. In 2006, he received a B.S. in Electrical Engineering and Computer Sciences as well as in Engineering Physics from the University of California, Berkeley. He went on to pursue a Ph.D. in Applied Physics at Cornell University under the guidance of Professor Jiwoong Park. He will continue his postdoctoral research at Columbia University with Professors Philip Kim and Abhay Pasupathy.

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CHAPTER 1

INTRODUCTION

1.1 Thesis Overview

Even though today our electronics industry is largely based on the semiconductor silicon, there has always been tremendous interest in studying the electrical properties of other materials. In the last few decades, materials derived from carbon have captured the attention of many researchers, not only due to the wealth of new science found in such systems, but for their potential use in electronics applications as well (*1-3*). Work in this area has been immensely broad. Specifically, we wish to focus on three carbon-based materials, for which at least one of the physical dimensions is predefined at the nanometer or even atomic scales. Such sizes are beyond what is achievable using current lithographic methods, and so these low-dimensional *nanomaterials* or *nanostructures* could be used to make extremely small and novel electronic devices (*4*).

At the same time, studies of electrical transport in low-dimensional systems exhibit two primary challenges:

i. *Transport behavior for nanomaterials can be very sensitive to changes in their local physical structure. In contrast, due to the advantage of sheer scale, the overall electronic properties of macroscopic systems are largely unperturbed by localized features.*

ii. *Nanomaterials must be electrically contacted by external metal electrodes, and so there may be significant transport barriers at the interfaces. While barriers also exist at metal contacts to bulk semiconductors, interfacial effects can be especially pronounced in systems with reduced dimensionality.*

In order to realize their full potential for future technology applications, such issues must be well-understood. However, transport measurements alone offer no spatial resolution, and so determining these effects will require the use of advanced microscopies at the nanoscale in combination with electrical studies. This is the unifying theme of our thesis. The main chapters are devoted to the discussion of novel characterization techniques that integrate light and electron microscopies together with transport measurements, allowing for spatially resolved studies of electrical transport in graphene, carbon nanotubes, and pentacene thin films.

In the next two sections, we will give a brief introduction to these three materials and some of their possible applications. We then discuss the two challenges mentioned above in greater detail, motivating the use of spatially resolved characterization techniques. Next, we review some of the existing tools and methodologies used for distinguishing spatial differences in the electrical properties of nanomaterials, as well as their virtues and limitations. Finally, we summarize the main ideas of this chapter and provide an outline for the rest of the thesis.

1.2 Carbon Nanostructures

Pure carbon exists in several different physical forms, or *allotropes*, the most well known of which is diamond, an electrical insulator. In contrast, graphite, another

common allotrope found in ordinary pencil lead, conducts electricity very well. Its structure consists of many loosely bound atomic sheets stacked on top of each other, a single layer of which is known as *graphene*. Monolayers of graphene were isolated for the first time in 2004 and can be considered intuitively as a template material, from which various other carbon allotropes can be geometrically constructed (Figure 1.1).

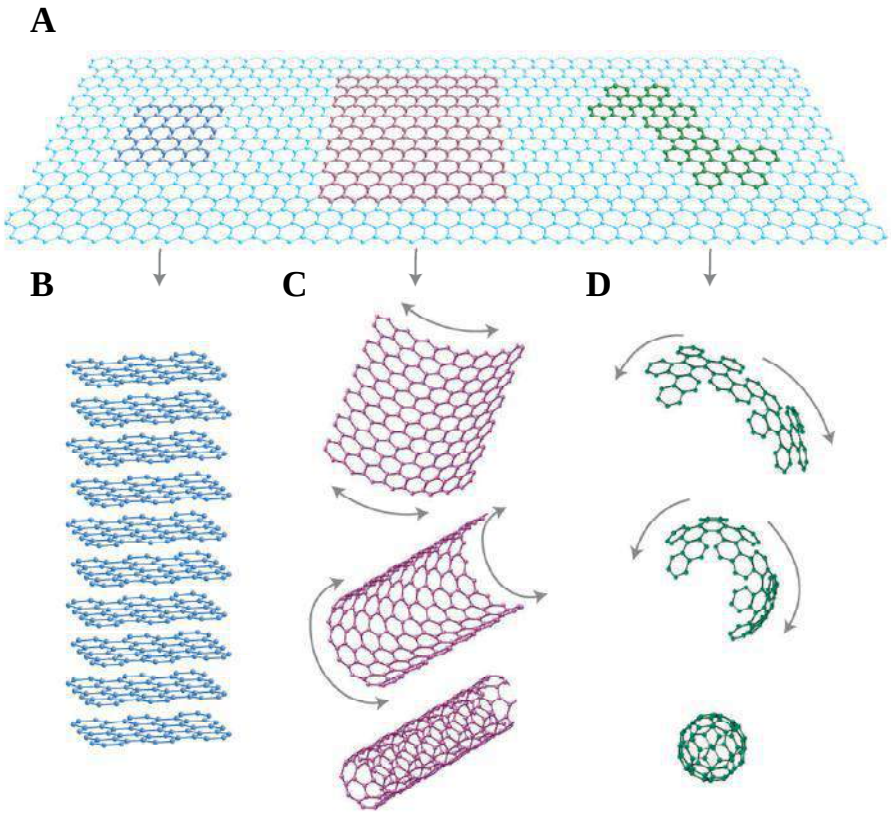

Figure 1.1 (A) Graphene as a template material from which carbon allotropes **(B)** graphite, **(C)** carbon nanotubes, and **(D)** buckyballs can be constructed. Adapted from (*5*).

Graphene

As shown in Figure 1.1A, graphene is composed of a honeycomb lattice of carbon atoms, each bound to three nearest neighbors. Since graphene is only one atom thick, we consider it to be a two-dimensional nanostructure. The electronic structure of

graphene shall be described in more detail in Section 2.2, but briefly, the orbitals of each carbon atom are sp^2 hybridized, leaving one set of π bond electrons delocalized and free to move above and below the plane of carbon atoms. Current carrying charges in graphene can travel with extremely high mobility, the most striking ramification of which is perhaps graphene's display of the quantum Hall effect even at room temperature (*6*). Unlike silicon, however, graphene is not a semiconductor, and so even though current flow can be tuned by electric gating, it cannot be turned off completely. This could ultimately prevent graphene from being used as the active material in logic transistors. Nevertheless, there is great excitement that graphene may find a role in radio frequency applications where a band gap is not necessary (*7*), as well as in large-area electronics (*8*).

Carbon Nanotubes

A different carbon nanostructure can be constructed when a single graphene sheet is rolled up into a cylinder (Figure 1.1C). These objects are known as *carbon nanotubes* and they were first discovered in 1991 even before the isolation of graphene. Depending on how they are rolled, their precise atomic structure and thicknesses may vary. Nevertheless, most nanotubes have a diameter close to 1 nm as well as aspect ratios significantly exceeding that of any other known material, effectively making them one-dimensional objects. Similar to graphene, carrier mobility in carbon nanotubes can be very large. However, as we shall discuss more carefully in Section 2.2, depending on the arrangement of the carbon atoms, nanotubes may be either metallic or semiconducting. This unique property makes carbon

nanotubes an extremely interesting material for fundamental study (*9, 10*). In addition, semiconducting nanotubes could potentially be used as transistors if their synthesis can be controlled (*1*).

Buckyballs

Finally, it should be mentioned that graphene can also be rolled up into a ball, forming a zero-dimensional structure known as a *buckyball* (Figure 1.1D). They were discovered in 1985 and are considered to be an interesting electronic material in their own right (*11, 12*), even though they are not the focus of this thesis.

1.3 Organic Thin Films

There exists another class of electronic materials whose study predates that of all the carbon nanostructures described above. In contrast to *inorganic* semiconductors such as silicon or germanium, materials derived from *organic* molecules may also be used to conduct electric current. Such molecules have carbon as a backbone, but do not consist solely of carbon like the allotropes previously introduced. Yet, similar to carbon nanotubes, they may be metallic, semiconducting, or even insulating depending on their precise chemical makeup (*13*). A gallery of famous organic semiconductors is shown in Figure 1.2A.

While a device made from a single molecule may represent the ultimate form of electronics miniaturization, the processing steps to make such a device are extremely difficult as well as unscalable. Furthermore, they have only been made successfully by a handful of groups (*3*). On the other hand, many scientists are able to

readily synthesize thin film structures comprised of many such molecules. Such *organic thin films* have properties that reflect those of the individual molecules and behave consistently down to just a few monolayers in thickness (*14*).

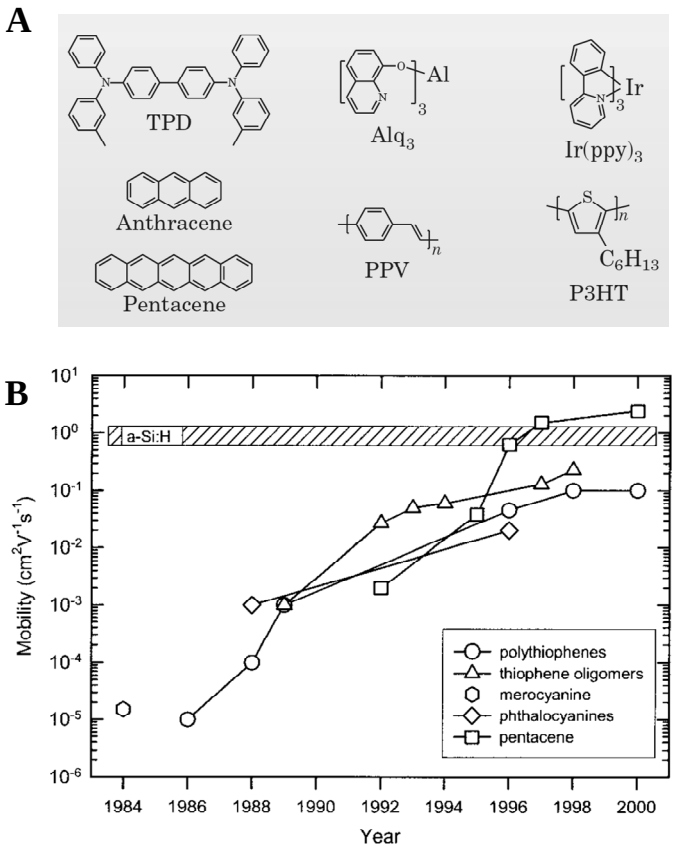

Figure 1.2 (A) Chemical structure of common organic semiconductors. Reproduced from (*15*). **(B)** Evolution of carrier mobility over time for several high-performing organic semiconductors. Reproduced from (*14*).

For electronics applications, the desirability of organic thin films derives from two main factors. First, unlike inorganic semiconductors, which are grown at very high temperatures, organics are produced at close to room temperature, and can often even be processed in solution. This results in substantial reductions to their cost, a primary motivation for their development. Second, the diversity of organic materials

far exceeds that of their inorganic counterparts, and so their properties can be vastly tuned via chemical synthesis. Unfortunately, in comparison to silicon or carbon allotropes, organic materials suffer from the general drawback of much lower carrier mobilities. Although this has improved dramatically over the years, at the moment, one of the highest performing organic semiconductors, *pentacene*, still trails silicon by roughly three orders of magnitude (Figure 1.2B). As a result, one also cannot expect organics to become the active electronic material in computing. Despite this limitation, they are already being widely used in select applications where high-mobility devices are not necessary, the most important of which include radio frequency identification tags and portable or flexible displays (*2*).

1.4 Electrical Transport in Nanoscale Systems

In the previous sections, we introduced two classes of low-dimensional, carbon-based materials that are actively being researched for both fundamental and technological motivations. When we make electronic devices from these nanomaterials, however, we find that transport can be keenly sensitive to their local structure as well as to the nature of their electrical contacts. We explore these two issues in greater detail below, using the example of carbon nanotubes as a model system for our discussion. For completeness, we first briefly review the Drude theory of macroscopic conductance in one dimension.

Conductance in One Dimension

In a large, rectangular conductor of length *L*, width *W*, and thickness *t*, the flow of electric current is governed by Ohm's law, which states that the current *I* flowing along its length is proportional to the voltage *V* biased across its contacting *source* and *drain* terminals (Figure 1.3):

$$I = GV = \sigma V\left(\frac{Wt}{L}\right). \tag{1.1}$$

The constant of proportionality *G* is the *conductance*, which, besides a dimensional factor, is determined by the material's intrinsic *conductivity* σ. One may also use the inverse quantities *resistance* $R = \frac{1}{G}$ and *resistivity* $\rho = \frac{1}{\sigma}$. This universal law dictates that two pieces of copper, for instance, will conduct current in the same manner when measured under the same experimental conditions, while gold is generally more conductive than tin.

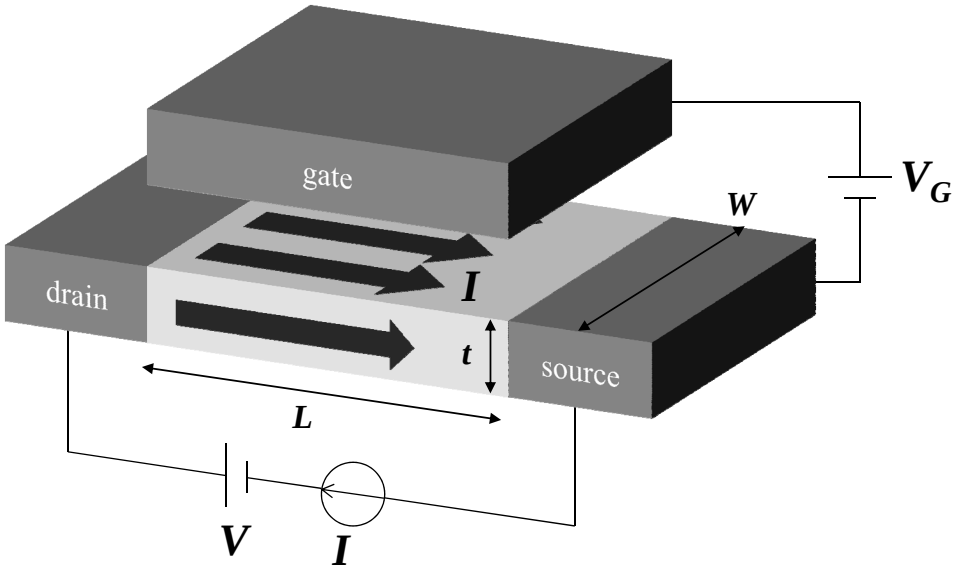

Figure 1.3 Schematic of a typical field-effect conductance measurement.

Conductivity is not a fundamental constant, however. It can be further decomposed into:

$$\sigma = en\mu, \tag{1.2}$$

where e is the electronic charge, n is the density of free charge carriers in the material, and μ is the carrier *mobility*, which describes how quickly each carrier can move under an electric field bias. In general, μ also depends on n, and so mobility should be specified for a given carrier density. Nevertheless, this relation tells us that the conductivity of a material may be tuned by changing either n or μ, or both. For a metal, the carrier density is typically very large and fixed, but its conductivity may still change with temperature T, as μ decreases with increasing T due more scattering between electrons and phonons.

For a semiconductor where the Fermi level is situated close to the band gap, the carrier density may be more readily altered. In particular, n increases with increasing T due to the thermal excitation of carriers. However, even at constant temperature, n may be adjusted upon the application of an external electric field. As shown in Figure 1.3, a third gate electrode can be placed in close proximity to the material and control for charge density via its capacitance C:

$$en = \frac{CV_G}{WL}. \tag{1.3}$$

Essentially, a gate allows for the conductance of an otherwise ordinary resistor to be electrically controlled by an external voltage V_G. This device geometry is called a field-effect transistor and will be used extensively in our discussions throughout. It is an important concept that lays the foundation for all of modern electronics.

Influence of Local Structure

When W or t shrinks to the scale of just a few atomic lengths, however, certain aspects of the above formalism break down. Namely, it is no longer informative to consider σ as a fixed parameter that is defined homogeneously across the sample. Instead, the local structure may play a crucial role in determining the overall electrical characteristics. It is important to note that for all the devices we encounter in this thesis, L is always macroscopic, and so we do not consider the *ballistic* regime where only G can be defined and not σ, although this is an even starker case where the Drude formalism loses validity (*16*).

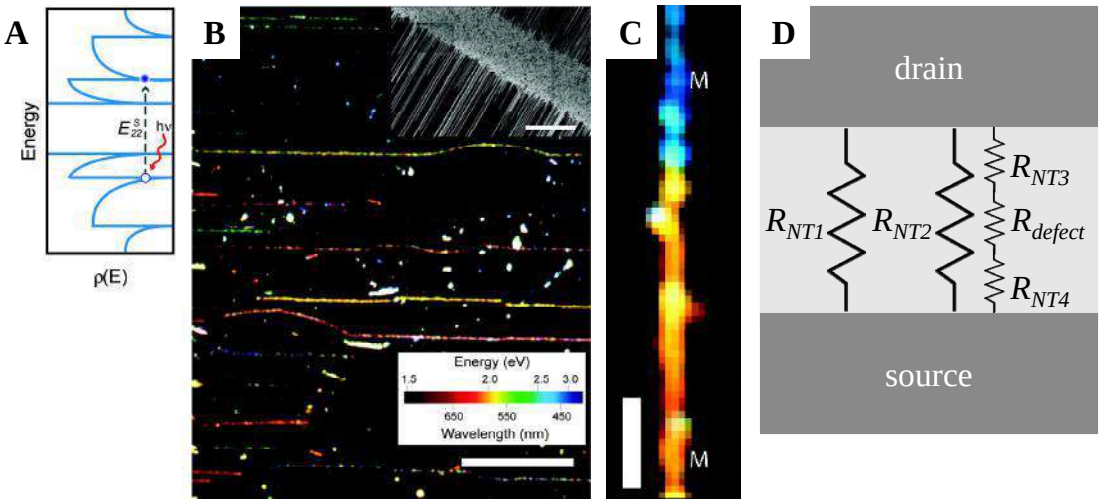

Figure 1.4 (A) Electronic joint density of states for a carbon nanotube probed by the Rayleigh scattering process. **(B)** Inset: SEM image of carbon nanotube array. Scale bar, 10 μm. Main panel: Rayleigh spectromicroscopy image of nanotubes. Scale bar, 20 μm. **(C)** Rayleigh image of a nanotube-nanotube heterojunction. Scale bar, 2 μm. Reproduced from (*17*). **(D)** Device with parallel nanotubes will only show ensemble characteristics.

The effects we mention can be clearly observed in carbon nanotubes, where $W = t$ is simply the nanotube diameter (≈1 nm). We have already mentioned that a carbon nanotube may be either metallic or semiconducting depending on how the underlying

graphene sheet is rolled up. In fact, nanotubes with different structures can exhibit a continuous spectrum of electronic behaviors, despite being composed of identical carbon atoms. In the inset of Figure 1.4B, we show a scanning electron microscopy (SEM) image of a dense array of carbon nanotubes on a quartz substrate that have grown out of a central strip containing a catalyst material. (We shall discuss the synthesis of nanotubes in more detail in Section 2.3.) One cannot resolve any structural differences beyond their lengths here.

Under Rayleigh spectromicroscopy (Figure 1.4B, main panel), however, one sees vast variations in their spectral characteristics, clearly distinguishing each carbon nanotube. Here, the colors represent the wavelengths that each nanotube scatters most strongly, and are a direct measure of the resonances in its electronic joint density of states (Figure 1.4A). Thus, within the energy range probed, nanotubes with different atomic structures can be clearly differentiated by the one or two resonant wavelengths in its light scattering. Such diverse electronic behavior knows no analog in bulk materials. In Section 2.2, we will show how this diversity will be directly manifested in the nanotubes' transport properties. In addition, we sometimes observe cases where defects produced during growth change the structure of an individual nanotube along its length (Figure 1.4C). These nanotube heterostructures will then exhibit the electrical characteristics of both sections, although the junction itself may impart new behaviors (*18*). In contrast, single defects and dislocations usually have little effect on the overall transport behavior in bulk systems.

Therefore, when one fabricates an electronic device consisting of even a few carbon nanotubes, it will exhibit transport characteristics that reflect only their

ensemble average (Figure 1.4D). Although we can still define an overall conductivity for the network, we lose knowledge of the diversity of behaviors exhibited by individual nanotubes. To account for the uniqueness imparted by their atomic arrangements, σ must be evaluated for each carbon nanotube locally.

Role of Contacts

For transport measurements, nanomaterials must be contacted with macroscopic metal electrodes, and so the nature of these interfaces can also strongly influence the overall electrical properties. In general, when making contact to semiconductors (bulk or nanomaterial alike), there will be a potential energy barrier, or *Schottky* barrier, for which charges must overcome for injection into the material. When the barrier is small, the contact is *ohmic* and current scales linearly with bias voltage as stipulated by Ohm's law. When the barrier is large, the current-voltage relation may be nonlinear. In nanomaterials, however, the length over which the barrier is effective could be much larger due to poor screening from their reduced dimensionality (*19*). This may lead to cases where contact effects alone dominate the overall transport properties of the device (*20*). Furthermore, for one-dimensional structures like carbon nanotubes, the precise atomic orbitals constituting the interface to the electrodes could also play an important role. For example, we often observe injection barriers even for metallic nanotubes, especially for those with smaller diameters (*21*).

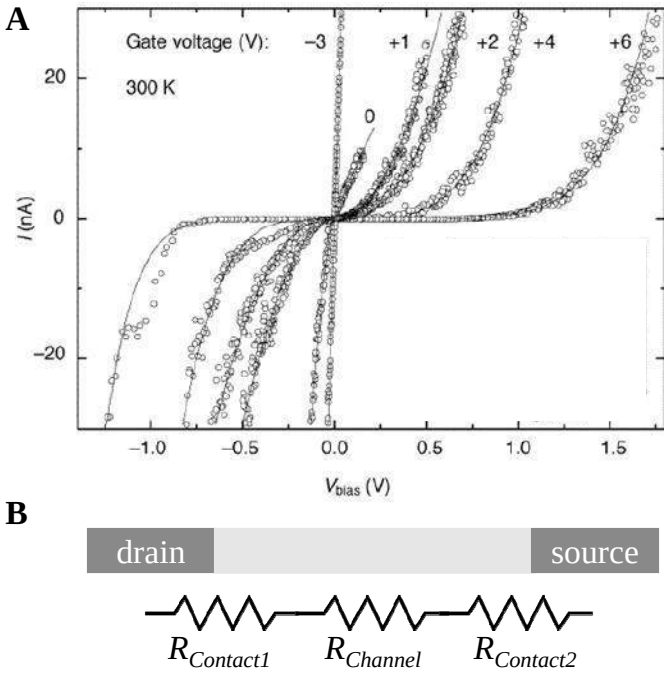

Figure 1.5 (A) Current as a function of source-drain bias for various gate voltages in a carbon nanotube transistor. Nonlinearity is attributed to Schottky barriers at the contact. Adapted from (*22*). **(B)** Phenomenological device model of contact effects.

In Figure 1.5A, we show example *I-V* characteristics from a field-effect transistor consisting of a single, semiconducting carbon nanotube. At negative gate voltage, the device exhibits clear ohmic behavior. Increasing the gate voltage, however, results in strong suppression of current at low bias and nonlinear behavior at high bias, indicative of Schottky contacts. The origin of this effect lies in the alignment and bending of the nanotube's electronic bands at the metal interface, a subject that will be discussed in Section 2.4. Phenomenologically, we may model all contact effects as resistances in series with that of the main body of the nanomaterial, or *channel* (Figure 1.5B), even though this does not necessarily elucidate their mechanisms, nor distinguish between the various internal electronic junctions that may form as a result of band bending.

1.5 Distinguishing Spatial Differences in Transport Properties

When the electrical behavior of a system changes depending on its local properties, due to either intrinsic structural differences or effects from the contact, a single conductivity parameter no longer provides the most informative description. This presents a great challenge to the complete understanding of nanoscale materials and devices. Most generally, we may consider conductivity or resistivity to be a spatially varying parameter to account for both effects. However, the typical conductance measurement (Figure 1.3) alone offers no spatial resolution, and so researchers have incorporated various microscopy techniques to address this need. We briefly review some general methods in this section, while a more thorough discussion will be reserved for the main chapters with reference to the particular nanomaterial under study.

Sequential Microscopy and Electrical Measurements

Currently, methodologies for spatially resolved transport studies can be divided into two categories. First, one may use microscopy to image the structure of a nanomaterial locally, and then lithographically address specific features for subsequent electrical measurements. Traditionally, this is done with tools such as SEM or atomic force microscopy (AFM). In the case of carbon nanotubes, for instance, one can use the AFM to determine the precise locations of individual nanotubes within a network in order to fabricate single-nanotube devices and study their characteristics locally. However, here the microscope plays only a passive role to aid in the lithographic process, and offers little insight on the material's structure

beyond topography. Furthermore, it may still be difficult to disentangle contact effects from the intrinsic properties of the nanomaterial itself, although one may use channel scaling to extract an average resistance for the contacts, provided that the channel is sufficiently long and uniform (*23*). Nonetheless, this procedure has become standard protocol in the study of nanomaterials, leading to many initial breakthroughs in their respective fields. Continuing with this methodology, in Chapter 7, we will introduce a new technique allowing one to electrically address nanomaterials after their structures have been fully analyzed by transmission electron microscopy (TEM).

Direct Imaging of Transport Properties

Alternatively, one can image the electronic mechanisms (electric fields, surface potential, etc.) directly for a nanoscale device *in situ*. The most popular methods used for this type of characterization are generally termed *scanning probe microscopy*. The oldest technique in this family is scanning tunneling microscopy, which can image electron density on the surface of conducting materials with atomic resolution and elucidate carrier scattering mechanisms. It can also be used in a spectroscopic mode to determine the local density of states as a function of energy (*24*). In general, however, the tool is not a direct measure of lateral transport properties.

The other scanning probe methods are variants of AFM, which can image the topography of any material, conductor and insulator alike, although usually not with atomic resolution. A schematic of the general technique is shown in Figure 1.6. Here, the force on a very sharp tip at the end of a flexible cantilever is used to sense and track the height of the surface. The tip can be scanned to probe for the local transport

properties of a device in several ways. First, one may use a conducting tip to directly contact an electrically biased nanomaterial in various locations along its length, measuring either voltage or current (*25*). When the tip is used for voltage sensing, the situation is similar to channel scaling measurements, and an average total resistance for the tip and electrode contacts can be determined. When probing for local voltage, the influence of contact resistance at the tip is eliminated as no current flows into this junction.

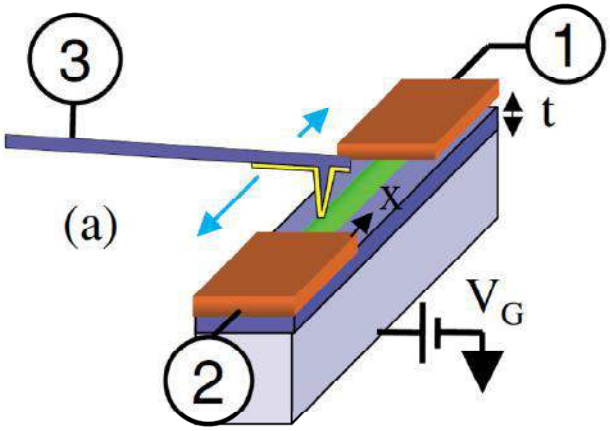

Figure 1.6 Schematic of AFM based measurement. Reproduced from (*25*).

It is inconvenient to have to make physical contact to the material every time in order to make a measurement. For both electrostatic force microscopy and Kelvin force microscopy, the tip can be made sensitive to the electric forces that arise from the local potential. Using these methods, one can then raster scan the tip to measure voltage at every location on the sample, generating true images of surface potential. This way, the voltage drops at the contacts may be clearly distinguished from that within the channel (*26*). Finally, the tip may be used as a local perturbation as well. In

scanning gate microscopy, a voltage is applied to the conducting tip as it rasters across an electrically biased device. The tip acts as a small gate electrode to modify the local conductivity as the overall current is imaged as a function of tip position. Areas with the greatest current change could indicate the presence of defects (*26*, *27*).

This suite of techniques provides a very powerful means to understand electrical transport in nanomaterials with spatial resolution. However, they suffer from three drawbacks. First, scanning probe measurements generally have small fields of view (≈100 x 100 μm) and are typically very slow—it takes long acquisition times to scan areas with high resolution. Second, the tip is most sensitive to the effects at the top surface of the material. Sometimes, the most interesting transport behavior occurs at the bottom surface that is in contact with the substrate, which is the case with pentacene thin-film devices. In other situations, the device surface may not even be exposed, but instead capped with a layer of another material, limiting the usefulness of scanning probe techniques. In Chapters 3 and 5, we will show how these two particular challenges may be overcome by using a scanning, focused laser spot in place of a physical tip.

1.6 Summary and Outline

In this chapter, we introduced three carbon-based materials that may potentially be used for future electronics applications: graphene, carbon nanotubes, and organic thin films. Although they have very different physical structures, all are considered to be nanomaterials since at least one of their physical dimensions is naturally defined on the nanometer or atomic scales. As a result, a full understanding

of their electrical properties is hindered by two significant challenges not similarly encountered in macroscopic systems. Namely, small changes in local physical morphology as well as in the nature of their electrical contacts may greatly alter device behavior. In order to optimize their electronic performance, one must then study their transport properties with spatial resolution. While scanning probe techniques already provide an invaluable toolset for this purpose, they suffer from a few limitations. In this thesis, we shall demonstrate two new techniques that may be used to understand spatial differences in electrical transport for these three carbon-based materials.

We first focus on carbon nanotubes. In Chapter 2, we will explain in greater quantitative detail how slight changes to the structure of nanotubes can yield diverse electrical characteristics. This property makes nanotubes fundamentally different from other electronic materials and presents a great challenge for the characterization of even a small network ensemble. While one can electrically address and study individual carbon nanotubes after a random synthesis, this procedure is extremely tedious and unscalable. Furthermore, it may be difficult to segregate effects from the contact from intrinsic transport properties. As a result, the integration of carbon nanotubes into relevant device technologies has been limited by the absence of fast and accurate spatial characterization methods. In Chapter 3, we introduce a photoelectrical technique based on a scanning, focused laser that can be used to image both electrical conductance and variations in band structure for individual carbon nanotubes in large, network device geometries, although we first demonstrate these measurements for single-nanotube devices.

We then use the same experimental scheme to study transistors based on pentacene thin films, one of the highest performing organic materials to date. Making good electrical contact to pentacene, however, remains one of the key challenges in the field. After introducing the basic properties of this material in Chapter 4, in Chapter 5, we show how photoelectrical microscopy can be used to not only image the *points* where pentacene are well-contacted to the underlying gold electrodes, but to determine the resistance of each contact point as well. Finally, we demonstrate a process for using graphene electrodes to make pentacene transistors with improved contact properties.

We lastly turn to the subject of polycrystallinity in graphene. In Chapter 6, we first discuss two primary methods for graphene production. We then describe how to characterize large-area graphene films over wide fields of view using dark field TEM, paying special attention to the structure of grain boundaries. These are the most prominent defect structures in the film and are predicted to exhibit dramatically different electronic properties than that of the pristine lattice. It is thus important to understand their impact on device transport. In Chapter 7, we use a novel experimental technique combining TEM with transport measurements to isolate and study the electrical properties of individual grain boundaries.

Chapter 8 will summarize all of these results as well as present some directions for future studies.

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CHAPTER 2

ELECTRICAL TRANSPORT IN CARBON NANOTUBE TRANSISTORS

2.1 Introduction

Single-walled carbon nanotubes (SWNTs) are cylindrical nanostructures that can be geometrically constructed by rolling up a graphene sheet seamlessly onto itself. In general, carbon nanotubes need not all be single-walled. Indeed, the first nanotubes discovered were multiwalled nanotubes, with many graphene layers forming concentric shells, bundled together in dense mats (*1*). However, recent advances in synthesis have made it possible to grow largely individual SWNTs directly on wafers using chemical vapor deposition (CVD) (*2*, *3*), and so we shall restrict our discussion to SWNTs in this chapter for simplicity. While all SWNTs are composed of the same honeycomb structure of carbon atoms, they can exhibit a myriad of different electronic structures. Depending on how the graphene sheet is rolled, they may be either metallic or semiconducting. Furthermore, the band gap of semiconducting nanotubes is a tunable quantity that changes with their diameter. These properties make SWNTs remarkably flexible as an electronic material that, ideally, can be tailored for specific applications.

Unfortunately, it remains a general outstanding problem to be able to controllably synthesize SWNTs of any particular orientation. As a result, for any ensemble of SWNTs produced, each will exhibit distinct electronic characteristics that

reflect its unique structure. In order to study their electrical transport properties, the nanotubes must then be isolated and characterized separated in individual device geometries, a tedious and unscalable process. When fabricating electronic devices with SWNTs, making good electrical contact to them could also be a challenge, as there may exist barriers to the injection of charge carriers at the metal-nanotube interface. In particular, contacting nanotubes with smaller diameters is especially difficult (*4*).

In this chapter, we will derive the electronic structure of SWNTs and show how it is directly manifested in the nanotubes' transport behavior. We then discuss the synthesis and fabrication of carbon nanotube transistors as well as their contact properties in greater detail. The challenges we encounter will set the framework for our spatially resolved photoelectrical measurements to be discussed in the next chapter.

2.2 Electronic Properties of Single-Walled Carbon Nanotubes

Since carbon nanotubes are rolled up graphene sheets, in order to understand their electronic characteristics, we must first understand the basic properties of graphene. We have already introduced the molecular structure of graphene in the introductory chapter. For this section, we shall derive its electronic band structure and show how it is intimately tied to the inherent symmetries in its crystal lattice. We then discuss the various electronic structures of SWNTs that can be obtained when graphene is rolled up. These behaviors are then reflected in the nanotubes' conductance properties when they are made into field-effect transistors.

Electronic Structure of Graphene

In graphene, the carbon atoms are arranged in a honeycomb structure, where the carbon-carbon bond distance is $a \approx 1.42$ Å (Figure 2.1A). The unit cell can be taken as the area enclosed by the dotted rhombus, with unit vectors $\vec{a}_1$ and $\vec{a}_2$. In momentum space, these structures transform to that shown in Figure 2.1B, with reciprocal lattice vectors $\vec{b}_1$ and $\vec{b}_2$. When we select the first Brillouin zone as the shape of the shaded hexagon we obtain three high symmetry points *Γ*, *K*, and *M*, the importance of which will soon become evident.

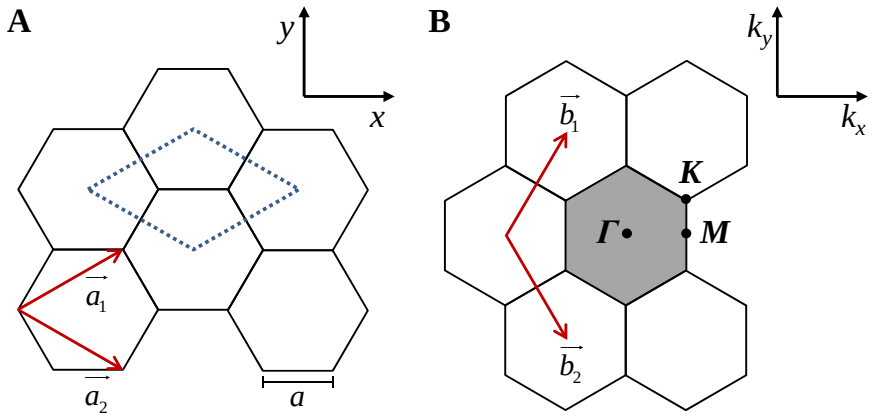

Figure 2.1 (A) Real space lattice of graphene with unit cell (dotted rhombus) and unit vectors labeled. **(B)** Reciprocal lattice with first Brillouin zone (shaded), reciprocal lattice vectors, and three high symmetry points labeled. Adapted from (*5*).

The atomic orbitals of the carbon atoms hybridize in the sp^2 configuration, leaving one set of p_z orbitals perpendicular to the graphene plane to form delocalized π bonds. These energy bands are responsible for charge transport in the material. To obtain their dispersion relation in momentum space, one can perform a tight binding calculation by considering only nearest neighbor interactions, with hopping energy $t \approx$

-2.7 eV. In this simplest approximation, the electronic band structure graphene can be described by (*5*):

$$E(k_x, k_y) = \pm t\sqrt{1 + 4\cos\left(\frac{\sqrt{3}k_x a}{2}\right)\cos\left(\frac{k_y a}{2}\right) + 4\cos^2\left(\frac{k_y a}{2}\right)} \qquad (2.1)$$

where $\vec{k}$ is the electron wave vector. A three-dimensional plot of these bands is shown in Figure 2.2A. The lower portion represents the bonding, or *valence* band, which is fully occupied in the limit of zero temperature and in the absence of external doping. The upper portion then represents the antibonding, or *conduction* band, which will be completely empty. We see that the two are maximally separated at the Γ point, but as we move away their gap decreases until the two bands touch singularly at the sixfold symmetric *K* (or Dirac) points, through which the Fermi level separating occupied and unoccupied states also passes. It can be further shown that the electronic density of states precisely vanishes here, making graphene a *semimetal*, or alternatively, a zero band gap semiconductor.

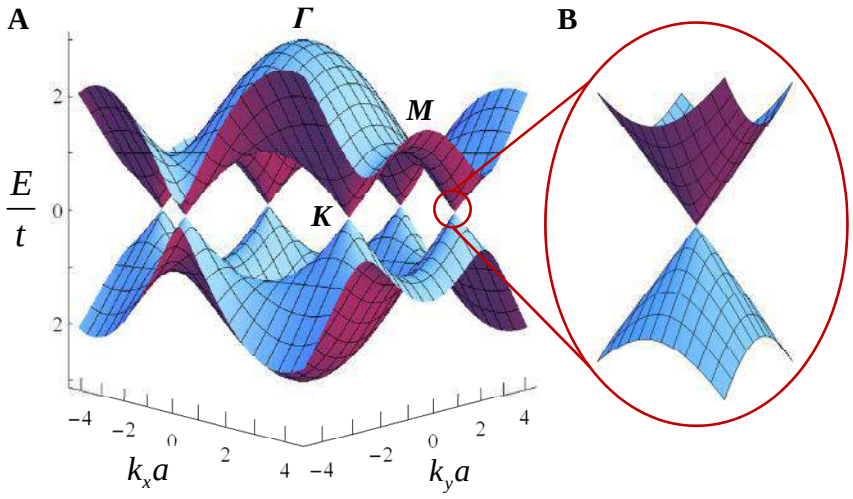

Figure 2.2 (A) Three-dimensional dispersion relation of graphene conduction (top) and valence bands. **(B)** Zoomed in plot of a *K* point. Adapted from (*6*).

The electrical properties of graphene will reflect its low energy band structure, and so we show a zoomed in plot of a Dirac point in Figure 2.2B. Locally here, the bands can be approximated to first order as:

$$E(\vec{k}) = \pm v_F k \tag{2.2}$$

where $\vec{k}$ now is the wave vector measured relative to the Dirac point, and $v_F \approx 10^6$ m/s is the called Fermi velocity. This dispersion relationship distinguishes graphene from most other electronic materials. In silicon, for instance, the energy bands scale quadratically with *k*, the curvature of which determines the effective mass of the electrons. Here, since energy has linear *k* dependence, electrons in graphene behave like massless relativistic particles, a topic that continues to intrigue many researchers (*7*). However, instead of traveling at the speed of light *c*, their velocity is given by $v_F \approx c/300$.

Electronic Structure of SWNTs

A SWNT can be viewed as graphene rolled into a seamless cylinder. Its structure may be described by a *chiral vector* $\vec{C} = n\vec{a_1} + m\vec{a_2}$ with integer indices (*n*, *m*) in terms of the unit vectors of graphene as base vectors (Figure 2.3A). The chiral vector connects two sites on the graphene lattice that become crystallographically equivalent once the carbon nanotube is rolled up, and is always perpendicular to the nanotube axis. The nanotube diameter is then simply $d = \frac{|\vec{C}|}{\pi}$. The angle of $\vec{C}$ relative to $\vec{a_1}$ determines another important parameter called the *chiral angle* θ. When $\theta = 0°$,

the nanotube is considered to be *zigzag* with indices (*n*, 0). When θ = 30°, the nanotube is *armchair* with indices (*n*, *n*). Otherwise, the nanotube is only *chiral*.

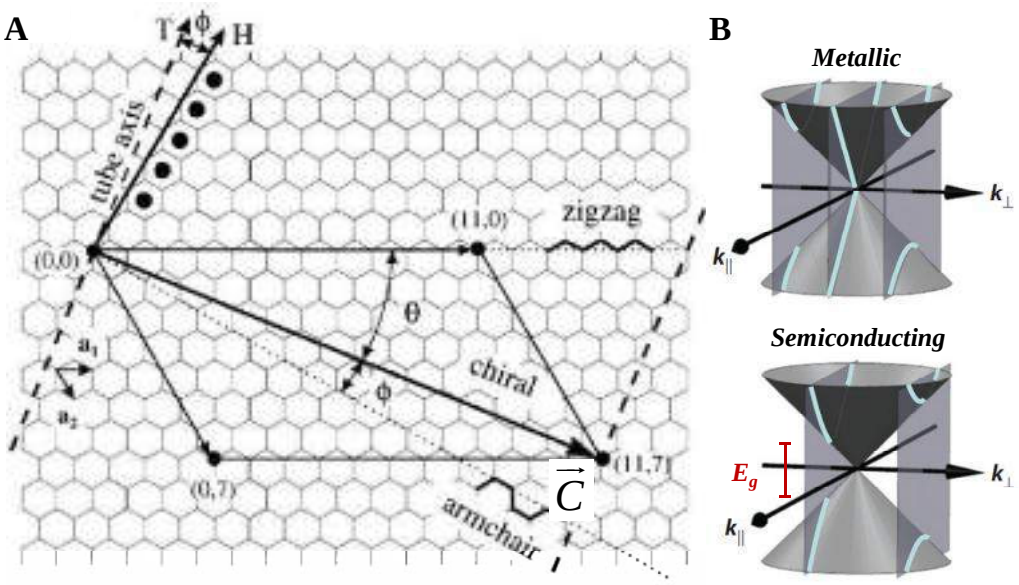

Figure 2.3 (A) Geometric construction of a SWNT from graphene. Reproduced from (*8*). **(B)** Band structure for metallic and semiconducting nanotubes. Reproduced from (*9*).

The electronic structure of SWNTs is keenly sensitive to its precise chiral vector. To see this, we observe that while the momentum wavevector along the nanotube axis $k_\parallel$ can take on a continuum set of values, periodic boundary conditions apply in the circumferential direction, quantizing $k_\perp$ under the condition $\left|\vec{C}\right| k_\perp = 2\pi q$, where *q* is an integer. As a result, the energy bands of a SWNT can be taken as a series of discrete plane cuts from the band structure of graphene with spacing 2/*d*. Each cut then becomes a different one-dimensional subband of the nanotube. If a cut happens to pass through a *K* point in graphene, the subband will have a linear dispersion relation at low energy with Fermi velocity $v_F \approx 10^6$ m/s, and the nanotube is metallic (Figure

2.3B, top). Otherwise, if all cuts miss the *K* points, the nanotube is semiconducting with a band gap E_g equal to that of the lowest energy subband (Figure 2.3B, bottom). It can further be shown that all armchair nanotubes have subbands crossing the *K* point, and are therefore metallic, whereas for other types (zigzag and chiral), we obtain metallic nanotubes only when $n - m = 3l$, where *l* is an integer (5). On average, one third of all geometries yield metallic nanotubes, while the rest are semiconducting. This amazing property of SWNTs is one of the key reasons for their appeal and intrigue, for no other material can have its electronic properties so widely altered with such small changes in atomic arrangement.

Electrical Conductance in SWNTs

A direct way to characterize the electronic properties of a SWNT is to measure its electrical conductance as field-effect transistors. The two general classes of SWNTs will exhibit distinctly different electrical behaviors in response to a gate field. For metallic nanotubes, the electronic density of states of the lowest energy subband is constant with respect to the position of the Fermi level, and so we do not expect their conductivity to change with gating. This is exactly what we observe in Figure 2.4A from their measurement performed at room temperature. Here, the total conductance *G* of the device is plotted as a function of gate voltage V_G. In contrast, the transport characteristics of a semiconducting nanotube are plotted in Figure 2.4B. When the Fermi level is tuned within the band gap, the device is insulating. It turns on for both electron (*n*-type) and hole (*p*-type) doping, although the conductance for *n*-doping is slightly reduced. As we shall see in Section 2.4, this is due to the presence of an

injection barrier for electrons at the contact. In the grayed regions where G scales linearly with V_G, we can extract corresponding values for electron and hole mobility in the nanotube from the slope, as $\mu \propto \frac{dG}{dV_G}$. Typically, one finds mobility determined by field-effect measurements to be in the range of 1,000 to 10,000 cm^2/Vs for nanotubes grown by CVD (*10*), roughly an order of magnitude larger than that for silicon, thus indicating that SWNTs are high-performance semiconductors.

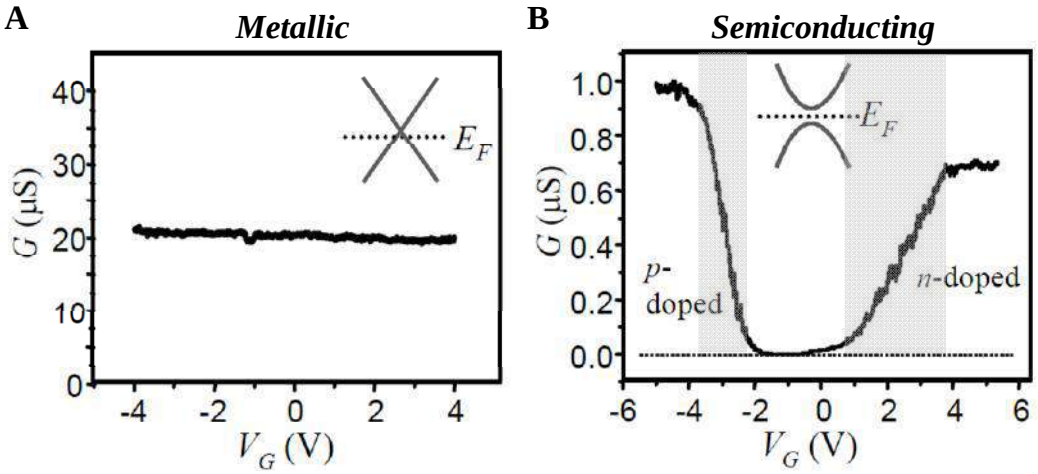

Figure 2.4 (A) Conductance of metallic nanotube is independent of gate voltage. **(B)** Conductance of semiconducting nanotube turns off when Fermi level is tuned within the band gap. Reproduced from (*11*).

While we haven't stated so explicitly, the energy band gap for semiconducting nanotubes is another structurally sensitive quantity which depends on the magnitude and orientation of the chiral vector. It can be shown that the value is inversely proportional to the nanotube diameter (*5*):

$$E_g = \frac{0.8 \text{ eV}}{d \text{ [nm]}}, \tag{2.3}$$

and so larger semiconducting nanotubes exhibit greater ambipolar behavior due to smaller E_g, whereas nanotubes with a wider band gap may only be able to conduct one carrier type within a certain gated range. This additional tunability further adds to the interest in carbon nanotubes as electronic materials.

2.3 Synthesis and Fabrication of Carbon Nanotube Transistors

We will now describe how carbon nanotube transistors are made. Since the device fabrication process varies depending on the particular synthesis method used, we will address both topics together in this section. We have already mentioned that there is yet no method to controllably grow carbon nanotubes of only a specific chirality, and so any synthesis technique will generally produce nanotubes of many random species, whose properties must be characterized afterwards.

Nanotube Synthesis

Initially, carbon nanotubes were discovered alongside much larger amounts of amorphous carbon and soot during an arc discharge (*1*). Since then, other routes for their production have been developed. Nanotubes can be grown in bulk quantities using either arc synthesis or laser vaporization techniques on graphite (*5*). These methods can produce SWNTs with large yields and of good quality. However, they are also usually entangled together in a dense mat, and must be dispersed before being cast on a wafer substrate for subsequent processing and device fabrication. Unfortunately, separation methods such as ultrasonication in a solvent are not completely effective, and leave many nanotubes bundled and even defective (*12*).

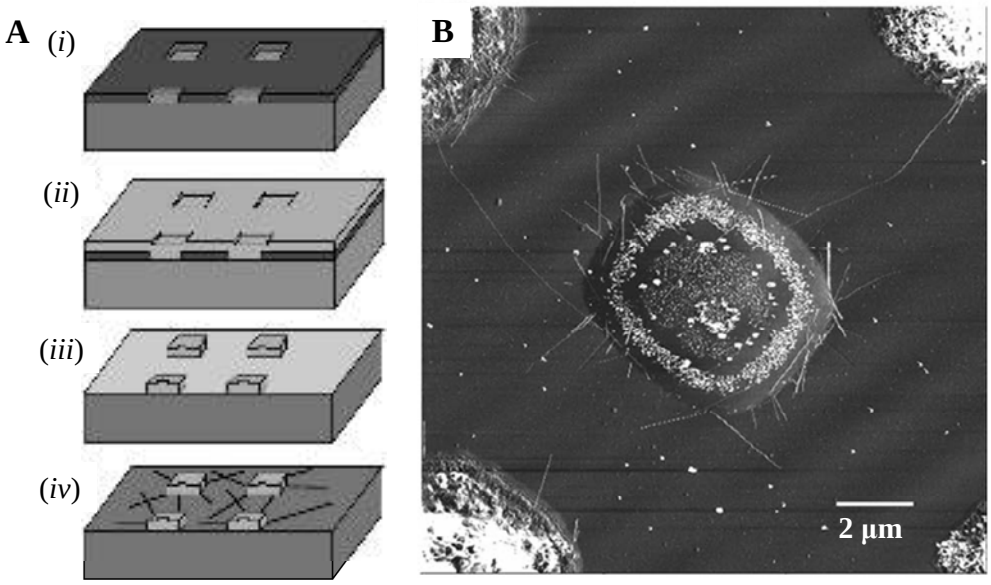

Figure 2.5 (A) Process flow for localized growth of carbon nanotubes from patterned catalyst islands. **(B)** AFM image of a catalyst island with nanotubes. Reproduced from (*2*).

Alternatively, it is possible to synthesize individual nanotubes directly on wafers using CVD. Their growth requires a catalyst, iron mixed with alumina nanoparticles for example, which must be first deposited on the substrate. From the point of view of device fabrication, this can be accomplished in two ways. Most simply, it is possible to disperse the catalyst in a solvent and then dropcast it globally on the growth wafer. CVD of methane will then produce an array of randomly oriented SWNTs, the density of which would depend on the density of nanoparticles in the dispersion. Alternatively, one might desire instead to limit the growth of nanotubes to predefined locations on the substrate. In this case, the catalyst could be placed in windows etched in patterned photoresist (*2*). After the solvent containing the catalyst is dried, one simply removes the resist in acetone prior to growth. A schematic of this process and an atomic force microscope (AFM) image of nanotubes growing

out of a catalyst island is shown in Figure 2.5. We use both these methods for the fabrication of nanotube devices in this thesis.

Finally, it has been demonstrated more recently that dense arrays of highly aligned SWNTs of excellent quality can be grown on single-crystal quartz substrates, also via CVD (*3*). While we do not utilize this process here, it is worth mentioning since the striking Rayleigh spectromicrosopy images shown in Section 1.4 consist of nanotubes synthesized this way.

Device Fabrication

Depending on whether the nanotube catalyst is randomly dispersed or localized on the wafer substrate, the device fabrication process could be very different. If single-nanotube devices are desired from randomly grown tubes, then the catalyst must be deposited on a substrate with prepatterned alignment marks. Individual nanotubes are then located via AFM, for instance, and electrically addressed using electron beam (e-beam) lithography. Usually, the substrate is a conducting silicon wafer with a layer of thermally grown silicon oxide on top, and so one can also use it as a global back gate. Most of the transport data on nanotubes that we have already shown come from devices fabricated in this manner.

The procedure is less time-consuming if one requires devices consisting of many nanotubes in parallel. In this case, a set of large electrodes may be patterned using conventional optical lithography on top of a randomly grown nanotube network. A schematic of this device concept is shown at the top of Figure 2.6A. At the bottom, we show an optical image of a large-scale nanotube device *L1* with two interdigitated

electrodes of 2 μm width and 8 μm spacing fabricated in this manner. Each quadrant is roughly 300 x 300 μm and the entire device consists of hundreds of nanotubes, although this number may be easily tuned by changing the catalyst density. We will show how to quickly find and characterize individual nanotubes in this device geometry using photoelectrical methods in Section 3.6.

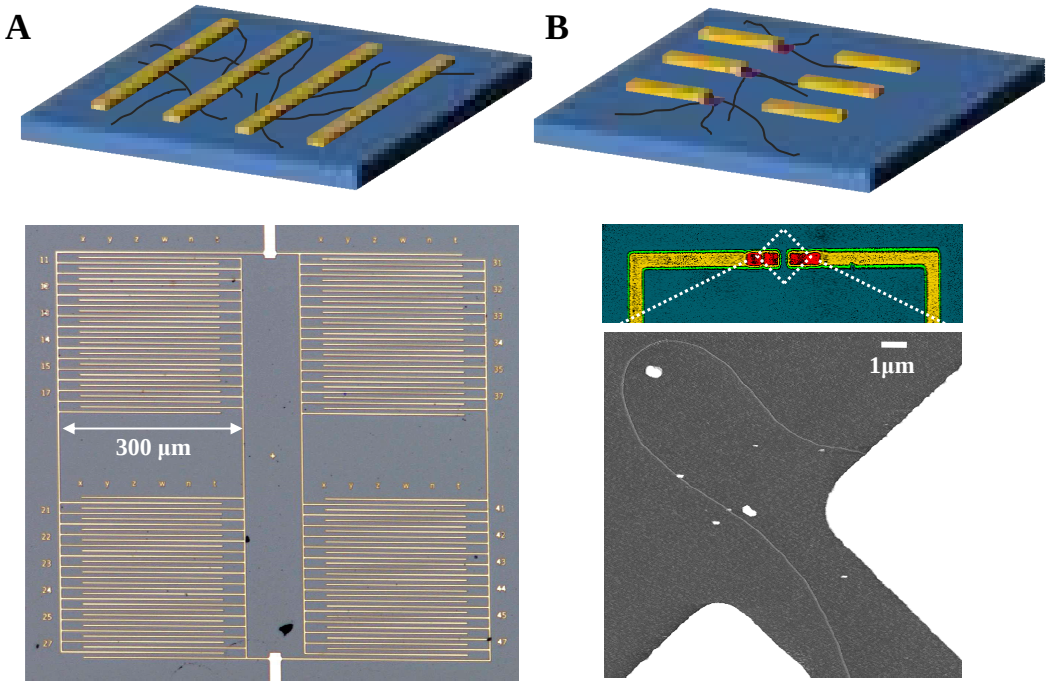

Figure 2.6 (A) Top: schematic of large-scale device concept fabricated from random nanotube synthesis. Bottom: optical image of large-scale nanotube device *L1* with interdigitated electrodes. **(B)** Top: schematic for individual nanotube devices fabricated from localized growth using patterned catalyst islands (purple). Middle: optical image of individual nanotube device *D1*. Red (yellow) denotes Pd (Au). Catalyst islands are not visible. Bottom: zoomed in AFM image showing a single carbon nanotube bridging the gap between electrodes. Adapted from (*13*).

Alternatively, one may localize the growth of carbon nanotubes by patterning islands of catalyst material on the substrate. While it is still possible to use e-beam lithography to address individual nanotubes in this case, a different method with

slightly higher throughput is available as well. In general, carbon nanotubes will grow out from the catalyst in all directions. However, it is assumed that a greater percentage will grow in the direction of the methane gas flow. Thus, with a second optical lithography step, one may pattern electrodes for each catalyst island using a geometry to maximize the probability of having one nanotube bridge the gap. Usually, this means that the end of one electrode overlaps the catalyst area and the other electrode is situated nearby (Figure 2.6B, top). All of our single-nanotube devices are fabricated using this method.

Nevertheless, one must then electrically probe the entire set of devices on the sample to determine which have nanotubes bridging them. Of the devices that conduct current, one must further determine via microscopy the number of nanotubes that cross the gap and contribute to conductance. On the bottom of Figure 2.6B, we show optical and AFM images of device *D1*, which consists of a single carbon nanotube with diameter ≈2.8 nm that has grown out from the catalyst to successfully contact both electrodes.

2.4 Injection Barriers at Metal Contacts

The conductance of carbon nanotube transistors is not determined by the intrinsic properties of the nanotube alone. In general, two types of barriers may be formed at nanotube-metal contacts to hinder the injection of charge carriers. The first is a physical barrier which reflects the degree of cleanliness of the atomic interface between the two dissimilar materials as well as the overlap of their electronic wavefunctions (*14*). If the metal cannot make adequate physical contact to the

nanotube due to poor wetting, then tunneling barriers are formed at the interface and can dominate device resistance (*15*). Gold and paladium are two common metals which have proven to make the best contact to nanotubes in this regard (*16*).

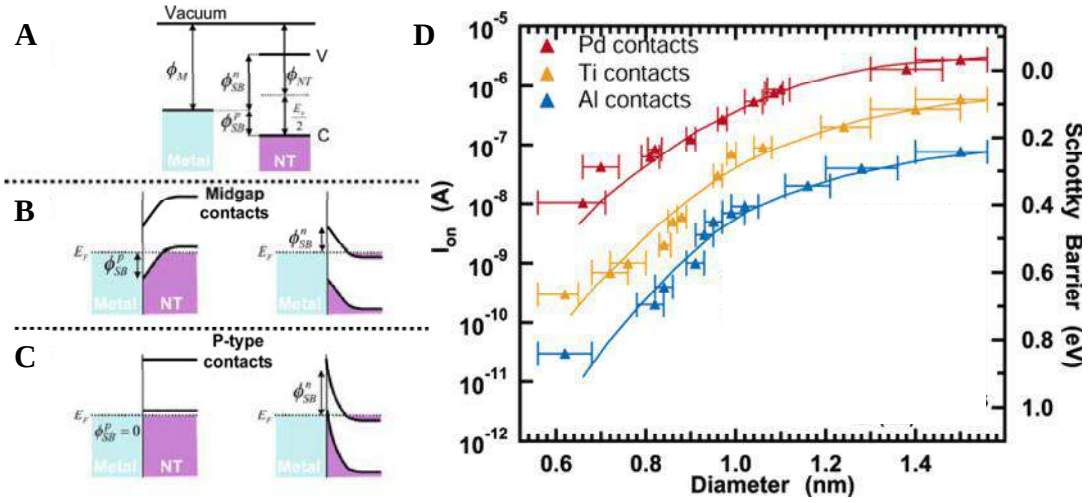

Figure 2.7 (A) Energy levels of metal and semiconducting SWNT before contact. **(B)** Band alignment when Fermi level of metal is within the SWNT band gap. The body of the nanotube can be made *p*-type (left) or *n*-type through field-effect gating. **(C)** Band alignment when Fermi level is within the SWNT valence band. Reproduced from (*14*). **(D)** On-state current (*p*-type) and Schottky barrier height for semiconducting SWNTs as a function of nanotube diameter for different three different contact metals. Adapted from (*17*).

A second, electronic barrier exists between metals and semiconducting nanotubes. In Figure 2.7A, we show the various energy levels of the metal and semiconducting SWNT in isolation. When the two are brought together, the bands are readjusted so that the Fermi level is flat and continuous across the interface at equilibrium. When the work function of the metal is such that its Fermi level lies within the nanotube band gap (Figure 2.7B), there will be Schottky injection barriers for both *p*-type (left) and *n*-type transport. However, when the metal work function aligns within the nanotube's valence band (Figure 2.7C), there will be no barriers for

hole injection (left), but a large injection barrier for electrons. Most common metals make *p*-type contact to semiconducting nanotubes, and so the asymmetric transport behavior we observed in Figure 2.4B can be explained by contact effects despite the symmetry of electron and hole bands in SWNTs near the Dirac point.

However, as we already mentioned, the band gap of a SWNT varies inversely with nanotube diameter, and so as semiconducting SWNTs get smaller, we expect Schottky barriers to form for hole injection regardless of the type of metal used. In Figure 2.7D, we show on state currents for *p*-type operation in semiconducting nanotubes as a function of their diameters for three types of metal electrodes. While palladium seems to make the best hole contacts overall, all currents decrease by several orders of magnitude as the diameter shrinks under 1.5 nm. Corresponding values for the barrier height are extracted using a self-consistent model. Although the formation of Schottky barriers is unique to semiconducting SWNTs, making ohmic contact to small nanotubes seems to be a general challenge, as even metallic nanotubes exhibit injection barriers when $d < 1$ nm (*4*). The precise origin of this effect is not completely understood. However, as the area of the metal-nanotube interface is reduced, the contact resistance could become very sensitive to the chemical bonding configurations of the junction, an area which deserves further exploration in the future.

2.5 Summary

In this chapter, we gave a detailed introduction to the subject of carbon nanotube electronics. We derived the electronic structure of SWNTs starting from that of graphene. We then showed how the diversity of their behaviors is directly

manifested in their transport properties. While large-scale devices can be easily fabricated using CVD synthesis of nanotube networks, it is not yet possible to controllably grow nanotubes of a specific chirality, and so each SWNT will exhibit unique electrical signatures that reflect its structure. For typical electrical measurements, this then entails the fabrication of transistors consisting of single nanotubes, which can be done either using e-beam lithography on randomly grown samples or optical lithography with a localized growth recipe. Both methods are extremely time-consuming as they require nanotubes to be located and characterized in a serial fashion.

Making ohmic contact to nanotubes is another challenge when studying their electrical properties. While metals like palladium and gold can be chosen to make devices with the best possible physical contacts, large electronic barriers to charge injection exist for nanotubes with smaller diameters. For semiconducting SWNTs, these are familiar Schottky barriers that result from band alignment. Surprisingly, injection barriers still exist for small metallic nanotubes, the origin of which is still largely unknown.

In the next chapter, we show how photoelectrical microscopy can be used to alleviate some of the difficulties with stand-alone electrical measurements and shed light on contact effects in nanotube devices as well.

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CHAPTER 3

IMAGING CONDUCTANCE AND TRANSPORT BARRIERS IN CARBON NANOTUBE TRANSISTORS

3.1 Introduction

In the previous chapter, we discussed how the two main challenges in studying nanoscale electronic systems are manifested for carbon nanotubes. First, since each nanotube is structurally and electronically unique, they must be characterized in isolation. Making single-nanotube devices is generally time-consuming as it requires the use of various microscopy tools, such as scanning electron microscopy or atomic force microscopy (AFM), to locate individual nanotubes either before or after the fabrication process. Second, it may be difficult to segregate the intrinsic properties of the nanotube from those of the transport barriers created at metal contacts.

Due to these issues, one should ideally possess the capability to quickly and directly characterize single nanotubes in an ensemble network without wiring them up individually. Towards this end, we now discuss our work enhancing bulk electrical measurements on carbon nanotubes with the resolution afforded by a focused laser beam. Using two different characterization modes, we were able to image both the electrical conductance and transport barriers in individual carbon nanotubes all in large-scale device geometries consisting of many nanotubes in parallel. To put these experiments in context, we first review some previous efforts on the imaging and

spatially resolved characterization of carbon nanotube devices. Many sections of this chapter are reproduced from (*1*) and (*2*).

3.2 Previous Work

Most of the more established methods to image transport in nanotubes come from scanning probe microscopy, the workings of which were briefly introduced in Section 1.5. Due to the spatial resolution afforded by the tip, one can isolate effects from different parts of the nanotube device. However, these methods usually have been applied to devices consisting only of individual nanotubes and bundles. The reason for this is twofold. First, multiple nanotubes create parallel current paths, the effects of which are difficult to disentangle even with such tools. Second, as scanning probe measurements are inherently slow and limited in their field of view, it takes long data acquisition periods to accurately image large-scale devices. In later sections, we will see how these two particular difficulties may be overcome with the use of a scanning, focused laser.

Electrostatic Force Microscopy

While a standard, two-terminal conductance measurement probes for channel resistance in series with that of the contacts, electrostatic force microscopy (EFM) may be used to map the potential along the length of the nanotube and segregate the two. At the top of Figure 3.1A, we show an EFM image of a device consisting of a multiwalled carbon nanotube with a resistance of 42 kΩ. The bottom plot shows that the potential drops linearly across the nanotube length with no abrupt changes at the

contacts. This implies that the device resistance is attributed mostly to the nanotube itself. The device in Figure 3.1B exhibits the opposite behavior. Here, the entire resistance of 40 kΩ is dropped at the contacts, as the potential is completely flat across the nanotube body. This implies that electrical transport within the carbon nanotube is ballistic on this length scale. These striking images give direct proof of the vastly different contact behaviors that may exist in carbon nanotube devices. However, more complete and quantitative measurements of contact resistance were obtained later on using the probe tip as a local voltage sensor (*3*).

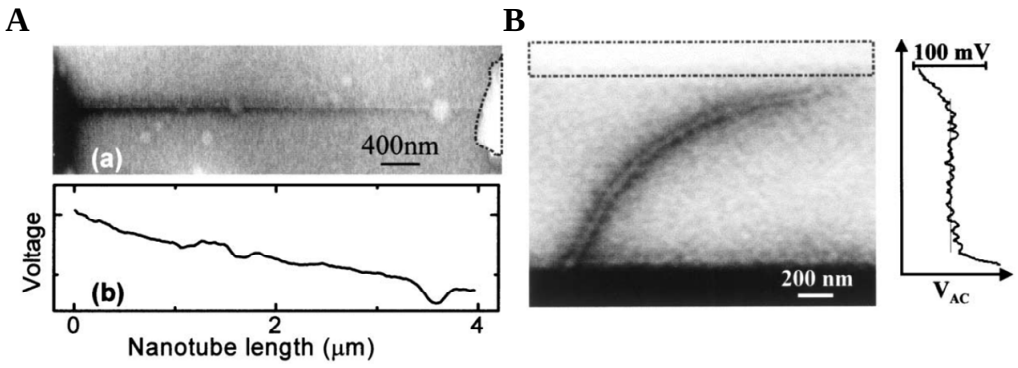

Figure 3.1 (A) Top: EFM image of surface potential in a multiwalled nanotube device. Bottom: voltage profile along the nanotube length, indicating minimal resistance at contacts. **(B)** Left: EFM image of a nanotube bundle. Right: voltage profile indicates that contacts dominate overall device resistance. Reproduced from (*4*).

Scanning Electrical Nanoprobe

For this measurement, the tip physically contacts a single-nanotube device at various locations along the nanotube length in order to detect the potential there directly. In particular, if one puts the tip very close to an electrode contact (≈100 nm away), the voltage drop will be primarily due to the contact resistance. In the inset of Figure 3.2, we show the overall conductance of a nanotube device with gold contacts

as a function of gate voltage, revealing the behavior of a semiconducting nanotube. In the main panel, the contact resistance R_S is plotted as a function of total device resistance R_T when the nanotube is doped *p*-type (black) as well as *n*-type (red). We see that contact resistance for hole doping is many times lower than that for electron doping. This suggests that the gold electrodes make *p*-type contact to the semiconducting nanotube, while electrons experience a Schottky barrier. Such results are consistent with our band alignment picture discussed in Section 2.4. Previously, however, contact resistance was not determined explicitly as spatial resolution was not afforded.

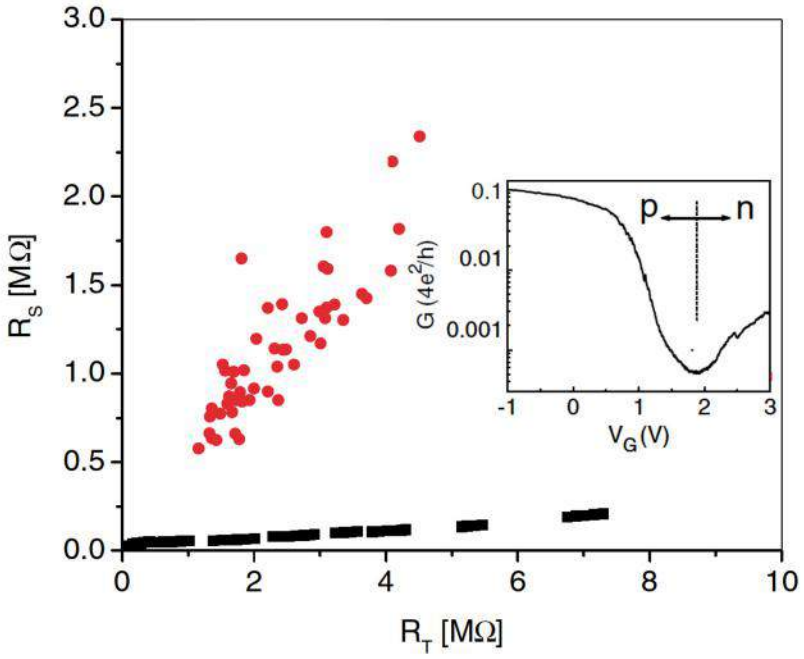

Figure 3.2 Inset: device conductance as a function of gate voltage indicating semiconducting nanotube behavior. Main panel: source contact resistance R_S vs. total device resistance R_T for *p*-type (black) and *n*-type (red) doping measured with tip contacting nanotube close to the source electrode. Adapted from (*3*).

Scanning Gate Microscopy

In scanning gate microscopy (SGM) measurements, a conducting tip acts as a movable gate electrode to modify the local conductivity of a nanotube device while the current is monitored as a function of tip position. It has been used to probe for defects in carbon nanotubes as they are expected to exhibit localized charging features (*4*, *5*). In Figure 3.3A, we first show an EFM image of carbon nanotube device with two kinks along its length. These features have been previously linked to defects in the nanotube (*6*). Large voltage drops are also seen to occur at these kinks indicating that they form resistive junctions. An SGM image of the same device is shown in Figure 3.3B. Here, strong spots of current enhancement are visible at the same locations, implying that the kink regions contain very low carrier density and constitute barriers to transport, consistent with their larger resistances.

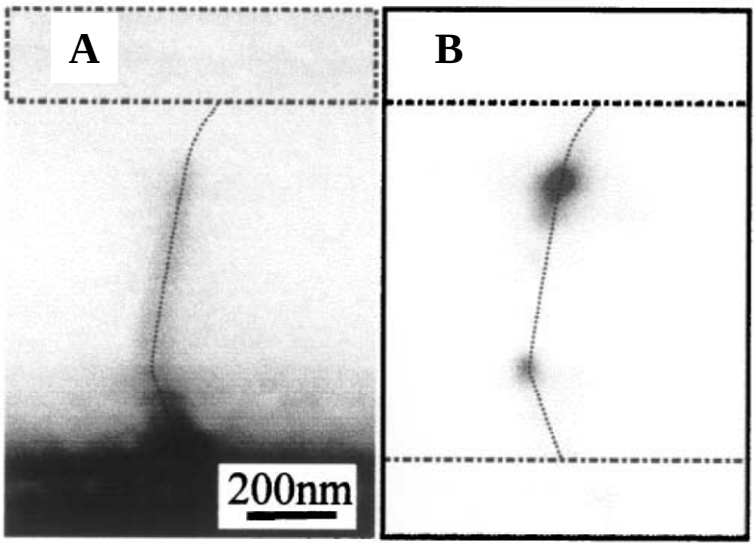

Figure 3.3 (A) EFM of nanotube with two kinks. Large voltage drops are seen across the kink junctions. **(B)** SGM image showing spots of enhanced current when tip gates kinked regions. Reproduced from (*4*).

3.3 The Scanning Photoelectrical Microscope

As typical electrical measurements on individual carbon nanotubes are slow and tedious, the ability to quickly image the electronic properties of individual nanotubes from a diversely synthesized network is a highly sought out goal. Unfortunately, scanning probe measurements on carbon nanotubes have still been mostly limited to the study of devices consisting of single nanotubes. In this section, we shall introduce a completely different imaging technique called *scanning photoelectrical microscopy* that can be used to characterize many nanotubes simultaneously.

The basic concept of photoelectrical microscopy is similar to that of SGM. In SGM, the tip acts as a movable gate electrode to electrostatically perturb the current at various locations in an electrically biased device. Here, we replace the tip with a focused laser to optically excite the current response. More specifically, a collimated laser beam with wavelength λ = 658 nm is incident on a pair of orthogonal scanning mirrors which direct it into a microscope. The beam emerges from the objective lens focused onto the device under study, whose terminals are electrically addressed for either voltage bias or current sensing. As the mirrors scan, the focal point of the laser is rastered across the sample, during which we monitor both the reflected light intensity and the current flowing through the device as a function of laser position. The current is measured using an amplifier, whereas the reflected light is detected with a photodiode and is used simply as a reference to determine the precise location of the laser spot, much like in ordinary confocal microscopy. To increase the signal-to-noise

ratio, one can also modulate the laser intensity and measure AC current using lock-in detection. A schematic of the entire apparatus is shown in Figure 3.4.

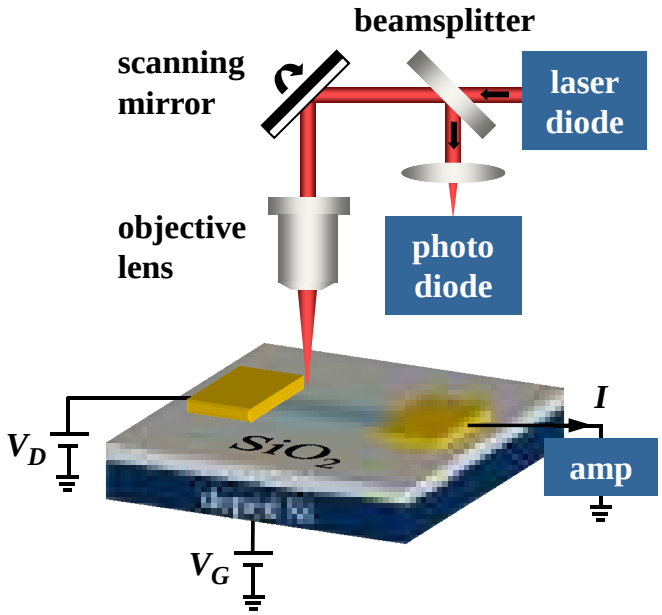

Figure 3.4 Schematic of the scanning photoelectrical microscope. Adapted from (*7*).

We can further separate photoelectrical measurements into two different characterization modes. First, the source and drain terminals could both be grounded, in which case one measures the intrinsic photogenerated current, or *photocurrent*, of the device. This would be a particularly meaningful measurement for *p-n* junction photodiodes, for instance (*8*). Alternatively, one can bias one of these terminals at constant voltage while sensing current from the other. This way, one measures the effect of the local laser excitation on the *dark* current already flowing through the device. This mode could be used to characterize effects such as *photoconductivity*. We will use both measurement schemes to examine our nanotube devices in the following sections, observing very different effects from each scheme. Finally, one can further

adjust the gate bias in all our photoelectrical measurements to determine the effects of charge density and doping.

3.4 Photothermal Imaging of Conductance

In this section, we describe how photoelectrical microscopy can be used to image for electrical conductance in individual nanotubes. To demonstrate and understand the mechanisms behind this effect, we limit our discussion to single-nanotube devices here for simplicity. In Section 3.6, we will show how the capabilities can be extended to characterize large-scale device geometries with hundreds of carbon nanotubes in parallel.

The Photothermal Effect

In the main panel of Figure 3.5A, we show in false color a current image of semimetallic nanotube device *D1* taken with $V_D > 0$ in AC mode with lock-in detection. An AFM image of this same device was shown in Figure 2.6B. We can see a strong current signal along the entire length of the nanotube. The reflection image is overlaid, so that the electrodes (outlined with dashed lines) are visible, and the circuit used in the measurement is shown for reference. The color at each point in the image represents the change in current ΔI measured in the device when the laser is incident on it. Comparison with the AFM image then suggests that device current changes when the laser spot is positioned on the nanotube. In particular, the polarity of ΔI is always the same throughout the device, maintaining its direction *opposite* to that of DC current, and so cannot be explained by photoconductivity. This effect is also

independent of bias polarity, strongly suggesting that the signal is due to a laser-induced conductance decrease in our nanotube device. In fact, the signal anywhere along the nanotube is found to scale linearly with V_D (Figure 3.5B), indicating that the conductance change $\Delta G = \frac{\Delta I}{V_D}$ is the fundamental quantity of interest in our measurement. Finally, the anisotropic laser polarization dependence of the current signal (Figure 3.5C) shows that the effect results from direct light absorption by the nanotube, as opposed to mechanisms that originate from the exterior, such as photoelectric gating (*9*).

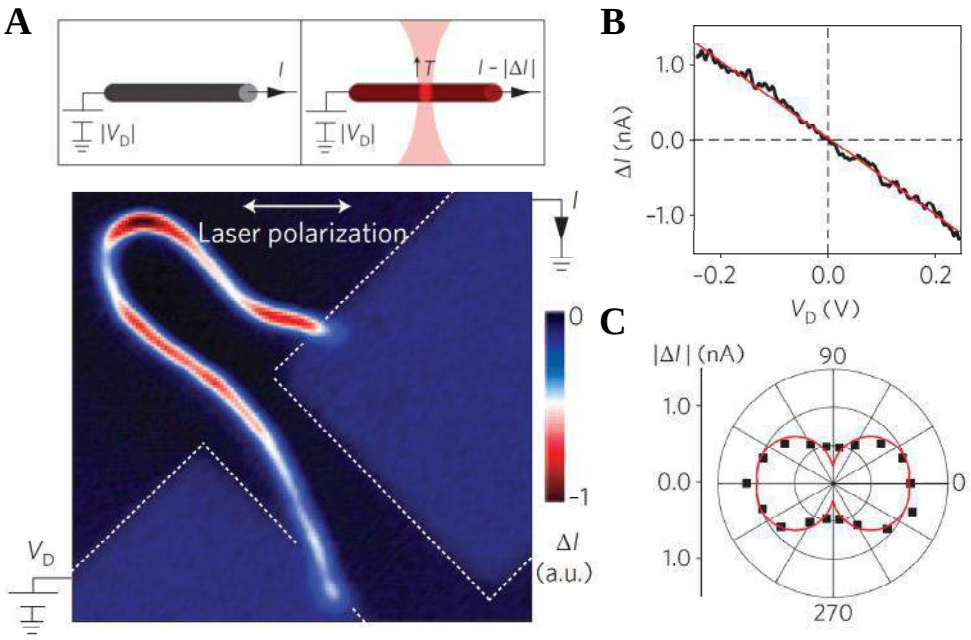

Figure 3.5 (A) Inset: diagram showing mechanism of AC current generation by laser heating. Main panel: current image of *D1* corresponding to $V_D > 0$. The measurement circuit, electrodes, and reflection image (overlaid) is shown for reference. **(B)** Bias dependence of current signal with laser fixed on nanotube. **(C)** Polarization dependence of current signal.

One direct way that light absorption can reduce the conductance of nanotubes is by increasing its temperature (*10*). Under applied bias, DC current flows continuously through the device. However, as the beam is scanned over the nanotube, a fraction of light power is absorbed and converted into heat, increasing the temperature of the nanotube. This then changes device conductance by amount ΔG and creates a current differential, or *photothermal current*, $\Delta I = \Delta G \cdot V_D$. Since we expect ΔG to be negative in metals (Section 1.4), ΔI is negative (positive) for positive (negative) V_D, as is the case in Figure 3.5B. In other words, the focused laser spot acts as a local heat source, while the nanotube device acts as a local temperature sensor. A schematic of this process is shown in the inset panels of Figure 3.5A.

Dependence on Device Conductance

We can describe the heat induced conductance decrease as $\Delta G = \left(\frac{dG}{dT} \right) \Delta T$, where T and ΔT are, respectively, the temperature and temperature increase of the nanotube, averaged along the nanotube length. The form of $\frac{dG}{dT}$ can be deduced from the reported temperature dependence of the electrical conductivity of carbon nanotubes, which is inversely proportional to temperature T near room temperatures for both metallic (*11*) and semiconducting nanotubes in the on state (*12*). Therefore, we can represent the total resistance of our device as $R = R_{int} \left(\frac{T}{T_{RT}} \right) + R_c$, where R_{int} represents the intrinsic resistance of the carbon nanotube at room temperature and R_c is the contact resistance, which is relatively insensitive to temperature (*11*). From this,

we derive $\frac{dG}{dT} = -\left(\frac{G}{T_{RT}}\right)\left(\frac{R_{int}}{R}\right)$. When the intrinsic nanotube resistance is the dominant factor (small R_c), this becomes $\frac{dG}{dT} = -\frac{G}{T_{RT}}$, whereas in the opposite limit (large R_c), we obtain $\frac{dG}{dT} = -\left(\frac{G^2}{T_{RT}}\right)R_{int}$. Based on this, we expect that ΔG will scale monotonically with G with a power dependence between 1 and 2.

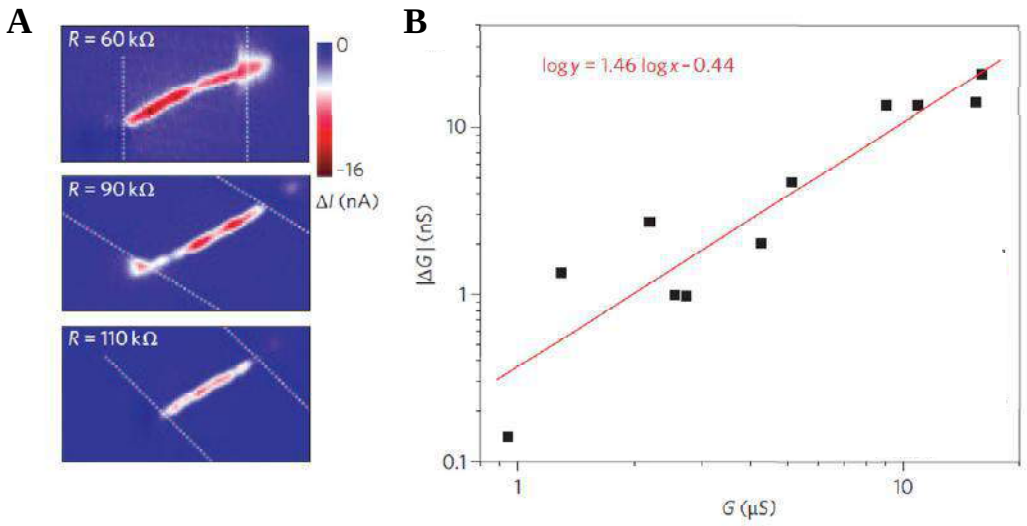

Figure 3.6 (A) Photothermal current images of carbon nanotube devices *D2*, *D3*, *D4* (resistances 60, 90, 110 kΩ) with V_D = 0.2 V. Electrode boundaries are marked with dotted lines. **(B)** Magnitude of laser-induced conductance decrease $|\Delta G|$, averaged over the nanotube length, vs. overall conductance G for 11 carbon nanotube devices in log-log scale and line of best fit.

Our measurements support this scaling. In Figure 3.6A, we show photothermal current images of three devices *D2*, *D3*, and *D4* with different resistances taken at identical bias and laser conditions. The photothermal current is overall largest (smallest) for the most (least) conductive device, a behavior that is universally observed. In Figure 3.6B, we plot $|\Delta G|$ (averaged along the nanotube length) vs. G in

log-log scale for eleven nanotubes measured under similar conditions. All nanotubes shown here have relatively large diameter (1.5 to 5 nm) and show metallic or semimetallic characteristics. We see that $|\Delta G|$ increases monotonically with G for over an order of magnitude, with the line of best fit revealing a power dependence of 1.46 ± 0.19, substantiating our prediction if we assume similar ΔT for these devices.

Dependence on Gate Bias

In general, the conductance of carbon nanotubes is dependent on the carrier density, which can be modulated with electric gating. In Figure 3.7A, we show photothermal current images of semimetallic nanotube *D1* at two different gate biases V_G = 0 and 5V. The overall current signal is clearly much stronger at V_G = 5V, suggesting that the nanotube becomes more conductive there. To study this behavior more quantitatively, we scan the laser at a fixed location along the nanotube and measure photothermal current simultaneously with G while continuously varying V_G. In Figure 3.7B, we plot $|\Delta G|$ (blue dots) and G (black solid line) as a function of V_G. We see that the two quantities track closely for all values of V_G. The odd dip in the transport curve at V_G < -3 V could be due to defects more prevalent at these nanotube lengths (*5*). For all metallic and semimetallic devices measured (≈10), we observe a close correspondence between the gate dependences of ΔG and G. In Figure 3.7C, we show similar plots for devices *D5* and *D6* that exhibit this correspondence at all gate biases, while their photothermal current images are shown in the insets.

We have also performed the same measurements on a semiconducting nanotube device *D7* with a well-defined band gap (Figure 3.7D). We see that the laser induces

photothermal current when the transistor is in the on-state at negative V_G (left inset), while the signal disappears altogether in the nanotube body once the device is off (right inset). Conductance is, however, *enhanced* upon laser illumination when V_G is tuned between the two regimes (middle inset). This conductance enhancement, which is strongest near the conductance turn off (see blue curve in the main panel), is likely due to a laser-induced thermal excitation of additional carriers (*8*), however further experiments will be necessary to examine additional effects, such as photoconductivity and photoelectric gating (*9*).

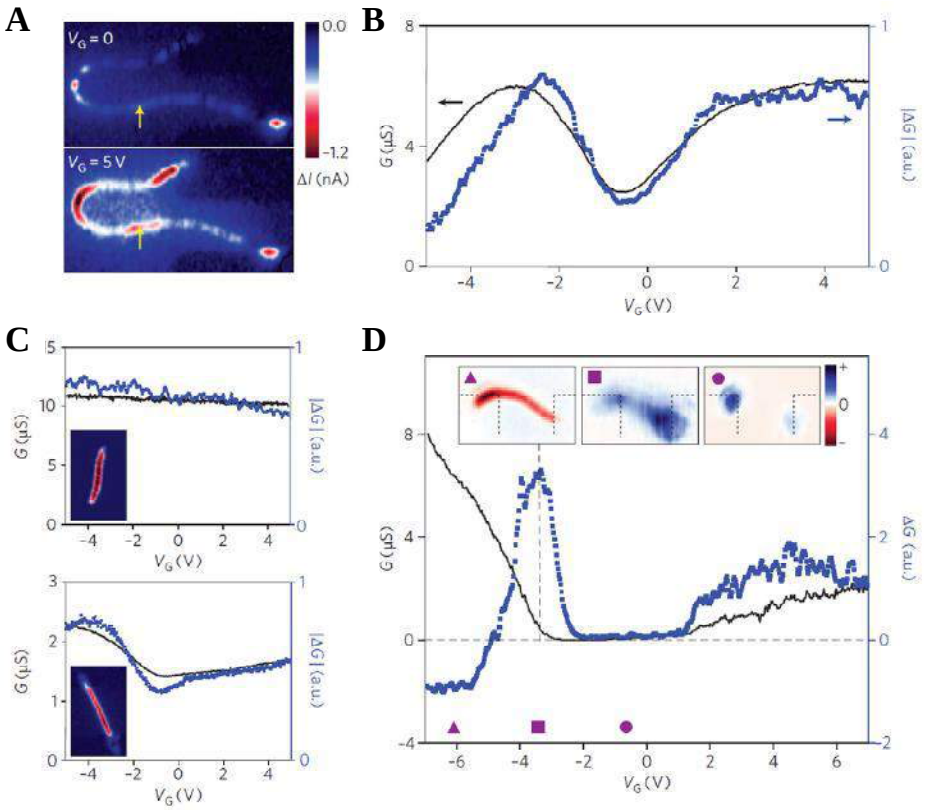

Figure 3.7 (A) Photothermal current images of semimetallic device *D1* with V_D = 0.2 V, V_G = 0, 5 V. **(B)** $|\Delta G|$ (blue dots), measured with laser fixed on the arrow shown in (A), and G (black line) vs. V_G. **(C)** ΔG, G vs. V_G for metallic and semimetallic carbon nanotube devices *D5* (top) and *D6*. Insets: photothermal current images of each device. **(D)** Same plot for semiconducting device *D7*. Insets: current images at different gate biases (indicated by corresponding markers).

To summarize briefly, in this section we have studied the effects of laser-induced heating on the electrical properties of individual carbon nanotubes. Since nanotube conductance is very sensitive to even local changes in temperature, we are able to use a focused laser as a heat source to image nanotubes with submicron resolution by detecting current differentials in the device. Furthermore, as photothermal current scales closely with device conductance, it can be used as an alternative probe for the electronic properties of the nanotube. While this may seem insignificant for transistors consisting of individual nanotubes, we shall see how it can be exploited to characterize large-scale devices with many nanotubes in parallel. But first, we will examine the intrinsic photocurrent response in unbiased, single-nanotube devices.

3.5 Photocurrent Imaging of Band Structure

In the previous section, a constant bias was applied across the source and drain terminals of the device driving a DC current through the nanotube. The laser light then modified this current via the photothermal effect. Here, we shall see that when we ground both terminals, the measured photocurrent becomes a probe of transport barriers within the nanotube.

Contact Photocurrent

In Figure 3.8A, we show the zero bias photocurrent image of the previous semimetallic nanotube device *D1* at $V_G = 0$, along with the circuit schematic used in the measurement. Here, instead of a uniform current signal seen along the length of

the nanotube, the strongest effects are seen at the nanotube-electrode interfaces, where we observe large photocurrent spots of opposite sign. We also see weaker signal from the nanotube body, which shall be discussed later. The mechanism responsible for contact photocurrent generation can be understood from Figure 3.8B, where we show the vacuum energy and Fermi level along the length of the device. While the relative position of the Fermi level in the nanotube body is controlled by the gate doping, close to the contacts they are controlled by the metal electrodes, causing bending of the bands at the interfaces. This results in strong electric fields driving photogenerated carriers in opposite directions at the two contacts.

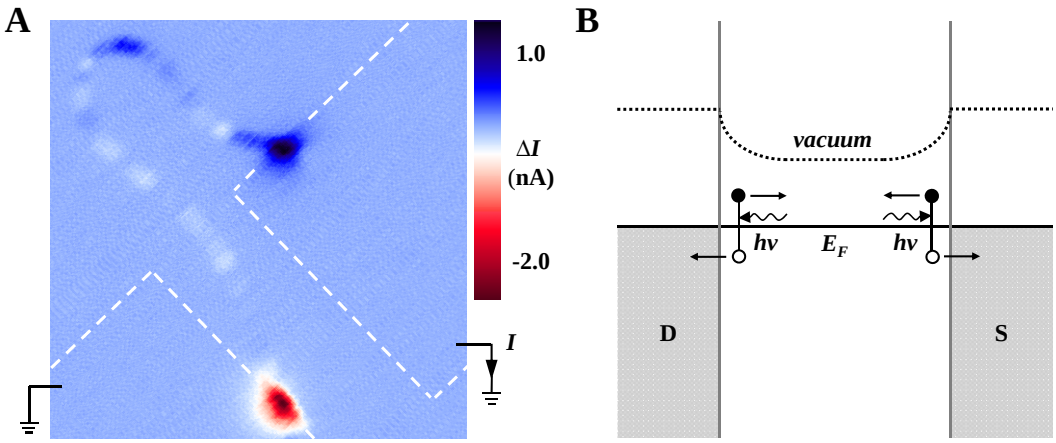

Figure 3.8 (A) Photocurrent image of device *D1* with $V_D = V_G = 0$. The circuit schematic and electrode outlines are shown for reference. **(B)** Mechanism of contact photocurrent generation in a metallic nanotube.

The Fermi level in the nanotube body can be tuned by changing the gate potential, and so we expect to be able to modify the photocurrent as well. More comprehensive measurements of this kind were performed on a semiconducting nanotube device, which we show in Figure 3.9A. The upper image shows the

photocurrent image of device *E1* measured at negative V_G. Again, we observe spots of opposite sign at the two contacts. The lower images show the gate dependent behavior of the photocurrent spots measured along the dashed line in the upper image as V_G is swept from -2.5V to 3.5V. Each spot vanishes at $V_G \approx 1$V and emerges with opposite sign. This behavior can be understood from the band structure diagrams in Figure 3.9B. At negative V_G, the entire nanotube is *p*-type, however the bands bend downward at the contacts. As V_G is increased, the bands in the nanotube body are pulled downward until they flatten across the entire length at $V_{G:FB} \approx 1$V, and photocurrent disappears. Continuing to increase V_G will make the body of the nanotube *n*-type, in which case the bands will bend upward at the contacts, changing the polarity of the photocurrent.

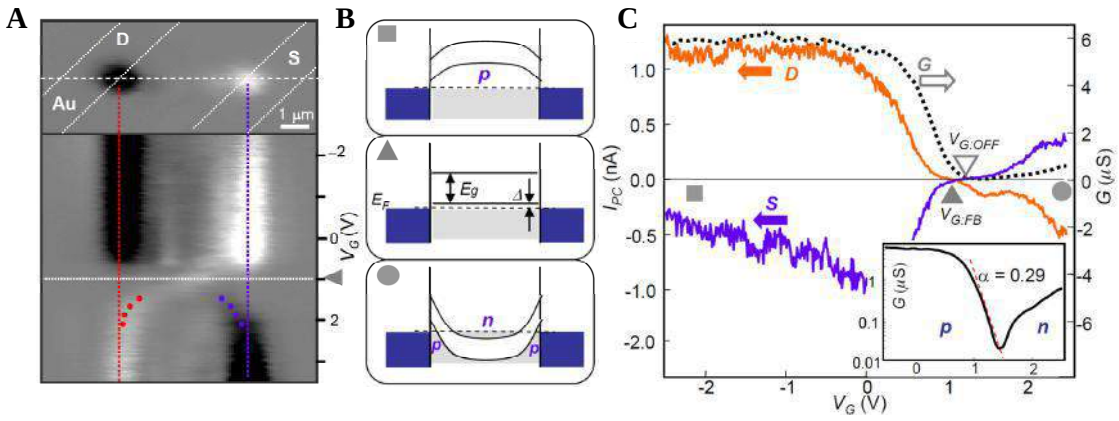

Figure 3.9 (A) Gate bias dependence of photocurrent in semiconducting nanotube device *E1*. **(B)** Band structure of *p*-type, flat band, and *n*-type cases. (C) Main panel: photocurrent at source and drain and overall device conductance vs. gate voltage. Inset: semilog plot of *G* vs. V_G.

A quantitative determination of the band alignment can be obtained when the photocurrent is measured in conjunction with overall device conductance (Figure

3.9C). In this plot, we see that as V_G is swept in the positive direction, the photocurrent for both contacts becomes zero slightly before the device conductance. Since the nanotube turns off when the Fermi level is aligned precisely with the valence band, the difference between these gate voltage positions determines the band alignment parameter Δ (see Figure 3.9B). We have $\Delta = \alpha e(V_{G:OFF} - V_{G:FB})$, where e is the electronic charge and α is the gate efficiency, which can be determined from the conductance near shut off (Figure 3.9C, inset) (*13*). For this particular device with gold electrodes, $\alpha = 0.29$ and $\Delta = 30$ mV. Thus, in contrast to EFM measurements which strictly probe for contact resistance, photocurrent microscopy can be used to spatially map the contact band structure, allowing for systematic studies on the effect of various metals and dielectrics to optimize for device performance, although that is not our focus here.

Influence of P-N Junctions

From Figure 3.9B, we expect there to be *p-n* junctions near the electrodes for electron doping, as only the main body of the nanotube turns *n*-type. Their presence should have a strong impact on the photocurrent behavior. In particular, a strong local electric field is expected at the *p-n* junction, with its maximum located at the center of the depletion region. Therefore, the peak photocurrent signal should also coincide with this position. In Figure 3.10A, we show line scans of photocurrent measured from *E1* in the *n*-type regime at various V_G. The most striking feature in this plot is the movement of contact spots as V_G changes. The peaks move away from the contact region (shaded area) and approach the middle of the nanotube with decreasing V_G. In

contrast, the spots in the *p*-type regime do not change throughout the whole gate bias range.

In Figure 3.10B, we measure both the photocurrent peak position and width as a function of V_G by using a Gaussian fit, which shows the peak movement with the same trend as described above. Surprisingly, the peak position moves more than 0.6 μm away from the contact, beyond which the signal is too weak for a precise measurement, while the width increases as well with decreasing V_G (Figure 3.10B, inset). We can understand both of these effects from the schematic shown in Figure 3.10C. As V_G increases, the main body of the nanotube becomes *n*-type when the intrinsic level of the nanotube E_i becomes lower than the Fermi level E_F. Because the contact region is still *p*-type, a large portion of the tube will form a depletion region. As V_G increases further, the position of the depletion region will move closer to the contact while its width W_D becomes narrower.

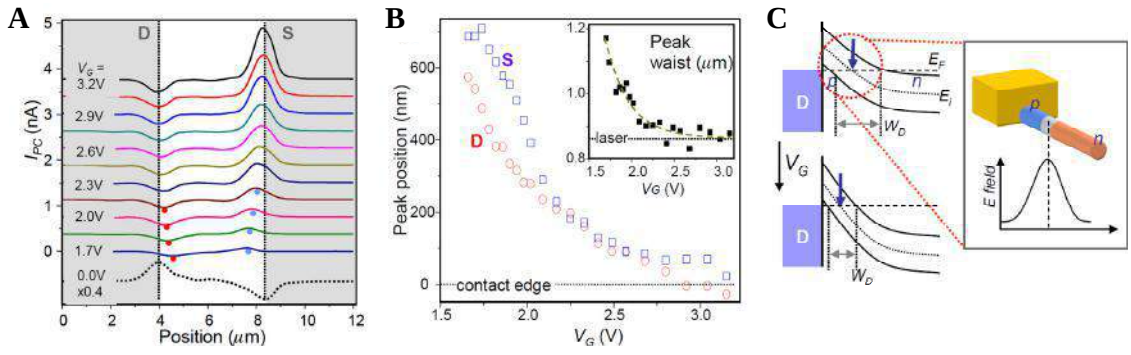

Figure 3.10 (A) Photocurrent line scans from *E1* in the *n*-type regime. **(B)** Main panel: photocurrent peak position vs. V_G. Inset: peak waist vs. V_G. **(C)** Schematic of *p*-*n* junction and depletion region (W_D) at different V_G.

Internal Transport Barriers

The combined results presented in this section demonstrate that zero bias photocurrent microscopy can be used as a very sensitive probe of the spatial variations in a nanotube's band structure. We now recall the weak photocurrent signal seen along the nanotube length in device *D1* (Figure 3.8A). We attribute this to local electric fields generated by transport barriers internal to the nanotube, the origin of which may be due to either defects or nonuniformities in the dielectric environment, although this can only be directly verified by other microscopic means. Nevertheless, we may try to obtain a qualitative understanding of the effect of these transport barriers on overall conductance.

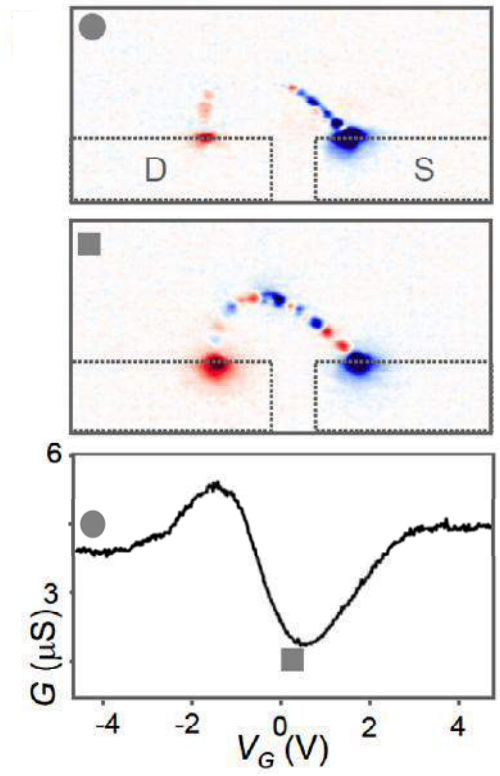

Figure 3.11 Bottom: conductance vs. V_G of semimetallic device *E2*. Top: Zero bias photocurrent images of *E2* at two different V_G as indicated by markers.

In the bottom panel of Figure 3.11, we plot conductance as a function of gate voltage for device *E2*. The behavior indicates that we have another semimetallic nanotube possibly with defects. Photocurrent images taken at two different gate voltages are shown in the upper panels. We see more and stronger photocurrent features along the body of the nanotube when the V_G is tuned to the point of lowest conductance, while many of the spots disappear when the nanotube is twice as conductive. This suggests that the transport barriers have a significant effect on the impediment of current flow. Photocurrent microscopy can then be used to locate these sources of disorder.

3.6 Large-Scale Photoelectrical Characterization

While photothermal imaging can be used to probe for the electrical conductance of carbon nanotubes, photocurrent is generated for both metallic and semiconducting nanotubes even when they are turned off. The two methods can thus be used as complementary techniques to image and characterize large-scale devices with many nanotubes in parallel. This is because each conducting pathway can produce an AC current upon laser illumination, and therefore, be probed separately with spatial resolution. As we have discussion in Section 2.3, large-scale nanotube devices can be synthesized more easily with random growth recipes.

For these devices, we can resolve the photothermal current for individual nanotubes if we use *heterodyne detection*. In standard lock-in detection, the laser intensity is modulated, the source-drain bias V_D is held constant, and current is measured at the laser modulation frequency. In heterodyne detection (Figure 3.12A),

both the laser and V_D are modulated, and current is measured at the difference frequency. This technique is preferred here since at fixed bias, the many conducting pathways will generate a very large DC current, preventing the detection of photothermal current from individual nanotubes amid the current noise. AC modulation of V_D eliminates the large DC current in our devices and improves the signal-to-noise ratio dramatically. A DC grounded bias T is used at the drain to further eliminate unwanted low frequency noise.

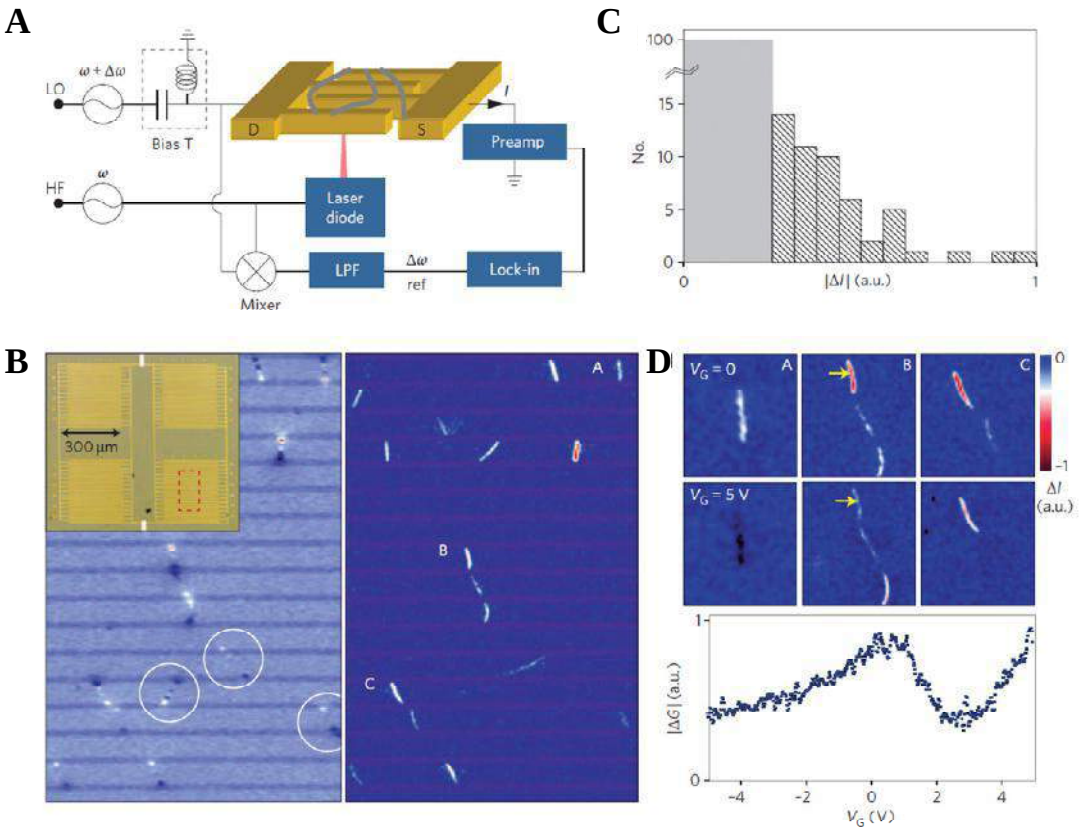

Figure 3.12 (A) Schematic of heterodyne detection setup and large-scale nanotube device under study. **(B)** Inset: optical image of large-scale carbon nanotube transistor *L1*. Right: photothermal image of the area outlined in red on *L1* taken using heterodyne detection with V_G = 0. Left: photocurrent image (V_D = 0) of the same scan area. **(C)** Distribution of photothermal current for over 150 carbon nanotubes from large-area scans. **(D)** Top: photothermal images of nanotubes *A*, *B*, *C* from (B) at V_G = 0, 5 V. Bottom: $|\Delta G|$ vs. V_G, measured with laser positioned at the arrow on nanotube *B*.

On the right of Figure 3.12B, we show a photothermal image taken of an area (marked in inset) on the previously shown, interdigitated device *L1* using heterodyne detection (V_G = 0). The reflection image is again overlaid so that the electrodes are visible. We can clearly see the photothermal current from many nanotubes, with the strength of each signal reflecting the conductance of each nanotube. A zero bias photocurrent image of the same scan area is shown on the left for comparison. While photocurrent is universally visible for most nanotubes, allowing us to locate contacted nanotubes regardless of their conductance, photothermal current will be stronger for more conductive nanotubes. Indeed, most nanotubes can be seen in both images while several that have clear photocurrent spots (circled in white) do not show visible photothermal current. We expect that these particular nanotubes are poorly conducting at this gate bias, and so their current signals are hidden within the noise floor.

Using this imaging scheme, we can qualitatively determine the relative conductance distribution for a large number of nanotubes. In Figure 3.12C, we show a histogram of the photothermal current observed for over 150 nanotubes from large area scans. The large bar at the far left denotes low conductance nanotubes that are not resolved from photothermal imaging yet are confirmed to exist through photocurrent scans. From our previous analysis, we believe that this plot should scale closely with the nanotubes' absolute conductances, although a more detailed study will be required to develop a technique with better quantitative information. It is also possible to determine the gate dependent conductance behavior of individual nanotubes in this array geometry by studying how their photothermal current changes with V_G. In Figure 3.12D (top), we show small area scans of nanotubes *A, B, C* from Figure 3.12B at V_G

= 0, 5 V, and we can see how each nanotube responds differently to the gate voltage. In particular, nanotube *A* disappears at V_G = 5 V, indicating that it is a semiconducting nanotube. We also see that different segments of nanotubes *B* and *C* contacting different electrodes behave distinctly as well. To obtain more quantitative information, one can fix the laser on individual nanotube segments and measure the photothermal current (or ΔG) while continuously varying V_G. In Figure 3.12D, we plot this for when the laser is on the top segment of nanotube *B*, revealing semimetallic behavior much like that seen in device *D1*.

The utility of photoelectrical microscopy is now fully apparent. By slightly altering our detection technique, we are able to study both the band structure and electrical conductance in individual nanotubes as a function of gate bias, although the device consists of hundreds of nanotubes in parallel and only two electrical leads. This capability would simply not be possible in bulk transport measurements nor using scanning probe techniques for the reasons already mentioned.

3.7 Summary and Outlook

In this chapter, we have discussed our work on the spatially resolved photoelectrical characterization of carbon nanotube transistors. The key motivation for these studies lies in the realization that current methods to electrically characterize individual carbon nanotubes are slow and time-consuming. In contrast, it is relatively facile to fabricate large-scale devices consisting of networks of carbon nanotubes, and so the capability to measure individual nanotubes quickly in such geometries is greatly desired. Photoelectrical microscopy could provide a valuable advance towards this

end. In particular, photocurrent imaging can be used to first map out the location of individual nanotubes in the network as well as to study their electronic band structures with spatial resolution. Photothermal characterization can then probe for the gate dependent conductance of each nanotube to determine its electronic orientation. The experimental setup involves only a simple microscope coupled with a laser source and a few basic electronic measurement units, further attesting to the ease and utility of the technique.

With minor modifications, we believe that photoelectrical microscopy can be used to investigate additional properties of carbon nanotubes, two of which are particularly noteworthy. i) We understand photothermal conductance to be $\Delta G = \left(\frac{dG}{dT} \right) \Delta T$. While $\frac{dG}{dT}$ is related to the nanotube's conductance, ΔT should depend on the amount of light absorbed by the nanotube. Therefore, by changing the wavelength of excitation, one may be able to obtain absorption spectra from photothermal characteristics. Since optical resonances are directly related to singularities in the joint density of states, this would be a further probe of a nanotube's electronic structure. ii) We often observe transport barriers in the body of long carbon nanotubes like *D1* and *E2* from photocurrent imaging, the origin of which we cannot clearly identify, although defects would be a very likely culprit. Unfortunately, this cannot be determined by photoelectrical measurements alone and must be verified by other methods, such as transmission electron microscopy (TEM) or light scattering microscopies (*14*, *15*). It would also be of great interest to study the effect of defects in nanotubes on its photocurrent properties by integrating photoelectrical measurements

with other microscopy techniques. For TEM, this can perhaps be done by using the methods discussed in Chapter 7.

Finally, photoelectrical characterization need not be limited to the study of carbon nanotubes alone. In the past several years, it has already been used to investigate other materials, such as graphene (*16*), germanium and silicon nanowires (*13, 17*), and of course, pentacene thin films (*7*), which we now proceed to discuss in the following two chapters.

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CHAPTER 4

ELECTRICAL TRANSPORT IN PENTACENE THIN-FILM TRANSISTORS

4.1 Introduction

Pentacene, one of the highest performing organic semiconductors, stands out as a prototypical material for the development of novel device geometries and characterization schemes. Furthermore, the field-effect mobility for pentacene thin-film transistors has improved by orders of magnitude over the years, making them much more relevant technologically (Figure 1.2B). One reason for this dramatic enhancement can be attributed to the structural optimization of pentacene films (*1*). We now understand that film morphology plays a determining role in device performance, with more highly ordered films giving better electrical characteristics overall. However, pentacene's bulk properties are not the only factor to affect device transport. Just like in other nanomaterials, charge injection into the film from external metal contacts is another process that must be optimized. When contact properties are taken into account, pentacene, in general, can only conduct hole charges, as the energy barriers for electron injection from most metals are too great to overcome. Yet, even efficient hole injection into pentacene films is not a trivial issue as often there is very large contact resistance in the device as a result of poor film growth at the metal interfaces.

As a prelude to the next chapter, where we study the contact properties of pentacene thin-film transistors using photoelectrical microscopy, here, we shall give a detailed introduction to the structural and electronic properties of pentacene films. We will also explain how pentacene transistors are fabricated, as the procedure must be specially tailored for the processing of organic materials.

4.2 Electronic Structure of Pentacene

While much of the following discussion has been widely known for many decades, it is necessary for a clear presentation of our original results. In brief, as direct consequence of its electronic structure, pentacene as a molecular solid is a wide band gap semiconductor. However, due to large injection barriers for electrons at metal contacts, it usually serves only as a conductor for hole carriers. This is similar to the case of semiconducting nanotubes with very small diameters.

Free Molecule

The structure of a pentacene molecule is shown in Figure 4.1A. It consists of five fused benzene rings (gray) bonded to hydrogen atoms on the periphery (white). The carbon-carbon bond length is 1.4 to 1.5 Å and the total length of the molecule is ≈14 Å. Recently, scientists were able to image this molecular structure with unprecedented spatial resolution using atomic force microscopy (AFM) at ultrahigh vacuum conditions and low temperature (Figure 4.1B). In the gas phase, a free molecule of pentacene has the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) positions at 6.4 and 2.3 eV below the vacuum

level, respectively, as have been measured from scanning tunneling microscopy studies (*2*). A band diagram along with the shape of the two orbitals is shown in Figure 4.1C. The very large HOMO-LUMO gap might seem to suggest that pentacene would not make a good electrical conductor.

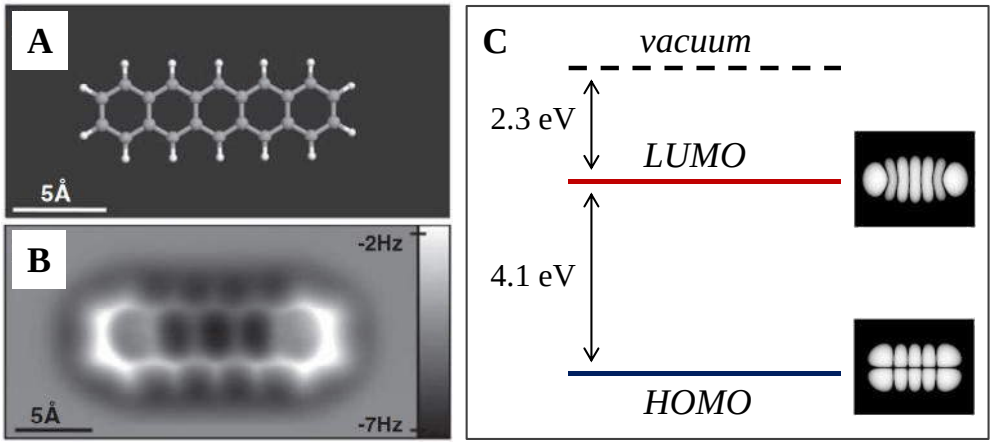

Figure 4.1 (A) Chemical structure of pentacene molecule **(B)** Atomic resolution AFM image of pentacene. Reproduced from (*3*). **(C)** Energy levels and HOMO and LUMO orbitals of pentacene free molecule. Adapted from (*2*).

Molecular Solid

The pictures changes in the molecular solid state. When many pentacene molecules are brought together, it is energetically favorable for them to assemble in the Herringbone arrangement, where the face of one molecule lies close to the edge of another. The structure of this bulk phase is shown in Figure 4.2A. The top view emphasizes the packing motive with unit cell parameters: a = 5.96 Å, b = 7.60 Å, and c = 15.61 Å, while the side view illustrates how subsequent layers stack on top of each other. For thin films, however, the arrangement of pentacene molecules could be different depending on the growth conditions. This will be discussed in Section 4.4.

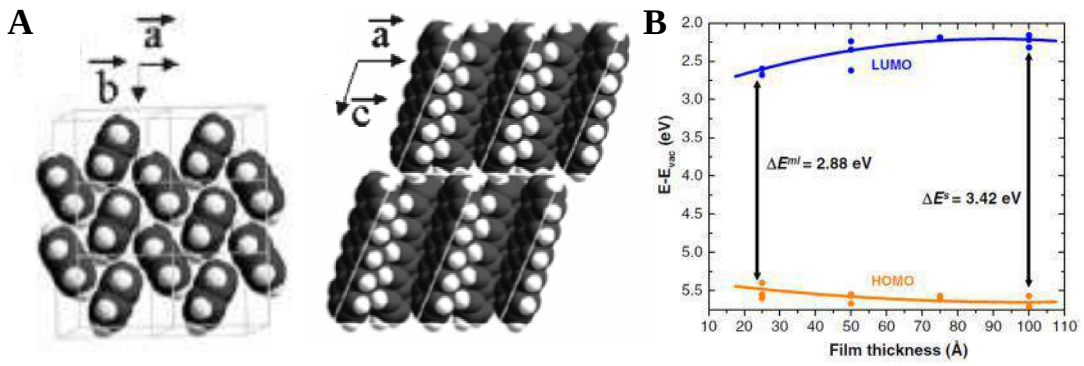

Figure 4.2 (A) Top (left) and side views of pentacene in the bulk phase. Reproduced from (*4*). **(B)** HOMO-LUMO gap as a function pentacene film thickness. Reproduced from (*5*).

In contrast to atomic solids like silicon or graphene which are covalently bonded, molecular solids are held together only by the Van der Waals force. As a result, the π electrons are still largely localized on each molecule, making most organic materials insulators. Pentacene, however, holds a unique place in this class of materials as electrons may be sufficiently delocalized across the molecular lattice, making it an efficient conductor in comparison. Furthermore, due to the interactions between molecules, bulk pentacene has a much smaller HOMO-LUMO gap of ≈3 eV when compared to the gas phase. This has been measured by direct and inverse photoemission studies (*5*), and we show the results as a function of film thickness in Figure 4.2B. The effective band gap for electronic transport, however, has an even smaller value of ≈2.5 eV, making pentacene a wide band gap semiconductor in the solid state.

4.3 Electrical Conductance in Pentacene Thin Films

Since the π electrons do not fully delocalize in organic materials as they do in inorganic conductors, the band picture of transport is not entirely applicable. Instead, conductance is actuated by a phonon-assisted hopping mechanism, where carriers constantly scatter as they travel between localized states (*6*). Charge mobility remains overall very low in such systems ($\mu \ll 1$ cm^2/Vs) as a result. Mobility in pentacene, however, is very close to this limit, and so the conduction mechanism may actually fall in between the hopping and band transport regimes. While the precise mechanism is still unclear, it is customary to borrow much of the language used for inorganic semiconductors in discussion of the transport behavior in organics, as it simplifies concepts considerably.

Band Alignment at Metal Contacts

The band alignment of organic semiconductors with metal contacts plays a key role in determining their electrical properties. In Figure 4.3, we show the band structure at the junction between neutral pentacene and gold, whose work function is W_f = 5 eV. At equilibrium, it has been found that an electric dipole forms at the interface, driving the vacuum level for pentacene 0.6 eV lower than that of gold. The resultant diagram reveals an effective energy barrier of Φ_h = 0.5 eV for hole injection into the tail of the HOMO band, and a much larger electron injection barrier of Φ_e = 1.2 eV. For this reason, pentacene is considered to be a *p*-type semiconductor, as it is difficult to inject electrons into the material.

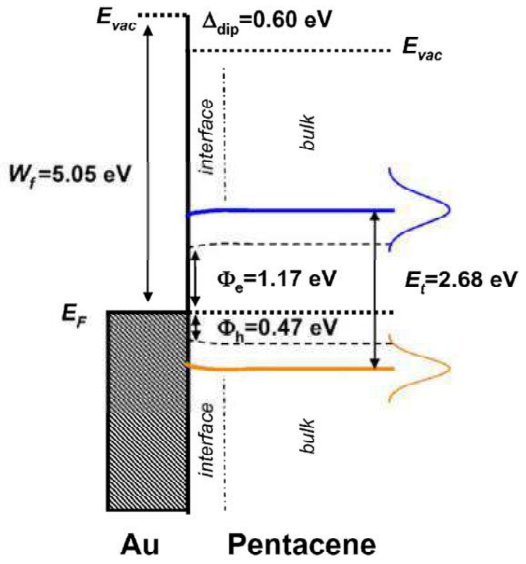

Figure 4.3 Band alignment of pentacene with Au metal contact. Reproduced from (*5*).

Transport Characteristics

These properties are reflected in the field-effect transport characteristics of pentacene thin films. In Figure 4.4A, we show typical *I-V* characteristics at several gate voltages from a pentacene transistor that we have fabricated—we shall delay discussion of film synthesis and device fabrication until the next section. When no gate field is applied, current is negligible at any source-drain bias, while for large negative gate values, current scales linearly with bias at first and then eventually saturates. These behaviors can be most clearly understood with reference to the series of diagrams in Figure 4.4B. Due to the large band gap, neutral pentacene is an insulator and must be doped to conduct current. Although one may try to dope pentacene *n*-type when $V_G > 0$, electrons cannot be injected from the metal electrodes due to the large energy barrier, and so the device is unresponsive. However, pentacene can be made *p*-type when $V_G < 0$ due to the lower barrier for holes. For a given $V_D < 0$,

current will then increase for larger $-V_G$ as the channel becomes more conductive. For a given $V_G < 0$, current scales linearly with $-V_D$ at first like any ordinary resistor. However, as $-V_D$ continues to increase, the area around the drain electrode eventually becomes undoped, and so current rises more slowly and eventually saturates when longer lengths of the channel is made insulating. This effect is called *pinch off*.

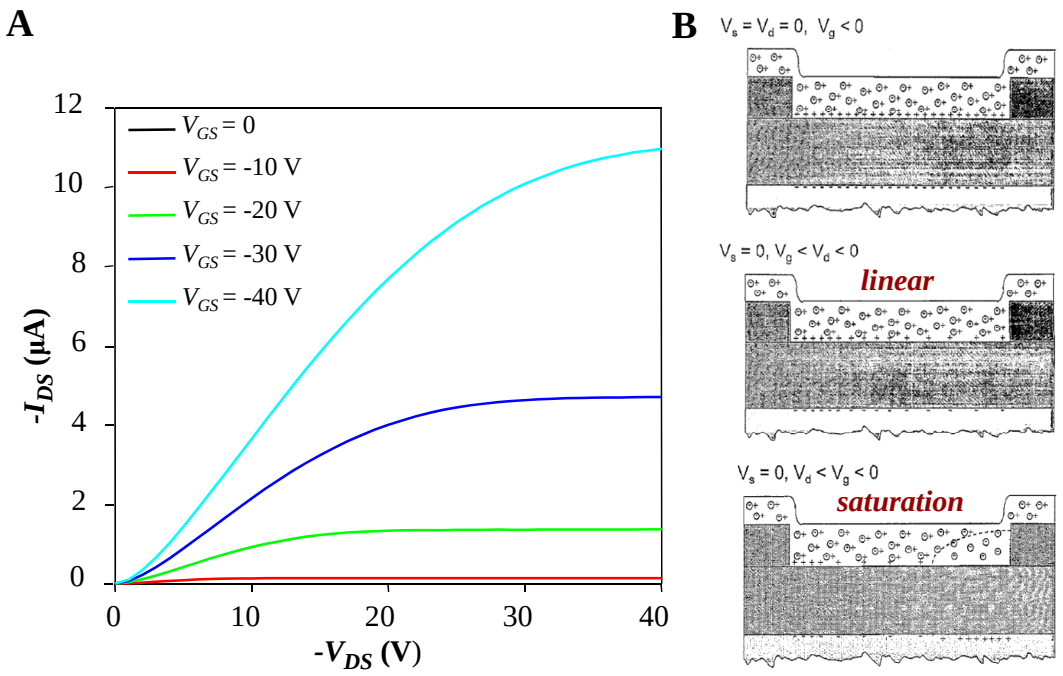

Figure 4.4 (A) *I-V* characteristics of pentacene thin-film transistor. $\mu \approx 0.2$ cm^2/Vs. Reproduced from (*7*). **(B)** Schematic of various transport regimes. Reproduced from (*8*).

In the linear region, current is described by (*1*):

$$I_D = \frac{W}{L} C\mu \left(V_G - V_T - \frac{V_D}{2} \right) V_D, \tag{4.1}$$

where W and L are the channel width and length, respectively, C is the capacitance per unit area of the insulating layer, V_T is the threshold voltage, and μ is the field-effect mobility. In the saturation regime $-V_D > -(V_G - V_T)$, we can model current as:

$$I_D = \frac{W}{2L} C\mu \left(V_G - V_T\right)^2 . \quad (4.2)$$

The mobility can thus be extracted from both regions, although it is usually slightly larger when calculated in saturation. For this device, we have $\mu \approx 0.2$ cm^2/Vs.

4.4 Synthesis and Film Structure

In this section, we will describe how pentacene thin-film transistors are made. In general, there are two common methods for synthesizing organic films, each with its own advantages and challenges. One can either dropcast the material in solution or evaporate it onto the wafer substrate in gas phase under vacuum. In either case, creating an ordered film is very important for obtaining good electronic properties.

Solution-Processed Films

One of the most attractive qualities of organics as electronic materials is that molecules can be processed in solution and then spun on the substrate. This is expected to have a very high impact on reducing manufacturing costs. Unfortunately, many small organic molecules are not easily soluble, including pentacene with its tightly packed Herringbone structure, although this could perhaps be improved through the use of heated solvents (*9*). Methods have also been developed to disrupt the packing of pentacene molecules by attaching them with bulky functional groups. This increases their solubility and has led to the successful fabrication of solution cast pentacene devices exhibiting relatively high electronic performance (*10, 11*).

Vacuum Evaporation

The traditional method to create pentacene films is to deposit them by vacuum deposition. Here, the organic material is heated to sublimation and the gas phase molecules are slowly evaporated onto a nearby wafer substrate. Very ordered films of high purity can be made this way. The technique also allows for precise control of the layer thickness; however, it does require the use of more sophisticated and expensive instrumentation in comparison with solution-processed methods. Since the pentacene films in our devices are made by evaporation in vacuum, we will limit the following discussion of film structure to those created in this manner.

Film Structure

The structure of a vacuum-deposited film, in particular that of the layers that are closest to the gate electrode, plays a dominant role in determining its electronic properties. This is because we require a highly ordered film where pentacene molecules are closely overlapped in order to conduct current efficiently via the field effect. The base pressure of the deposition system and deposition rate can both be widely varied to obtain an optimal film quality. Generally, higher vacuum implies longer mean free path of the sublimed molecules and fewer contamination. The purity of the source material is also very important. In addition, the conditions of the substrate during deposition can greatly influence the structure of the first monolayers of the film. On clean metals, pentacene molecules generally tend to grow with their benzene rings facing parallel to the substrate in the so-called *single-crystal phase* (*4*).

On inert surfaces like silicon oxide, the film structure is highly sensitive to the temperature of the substrate during deposition.

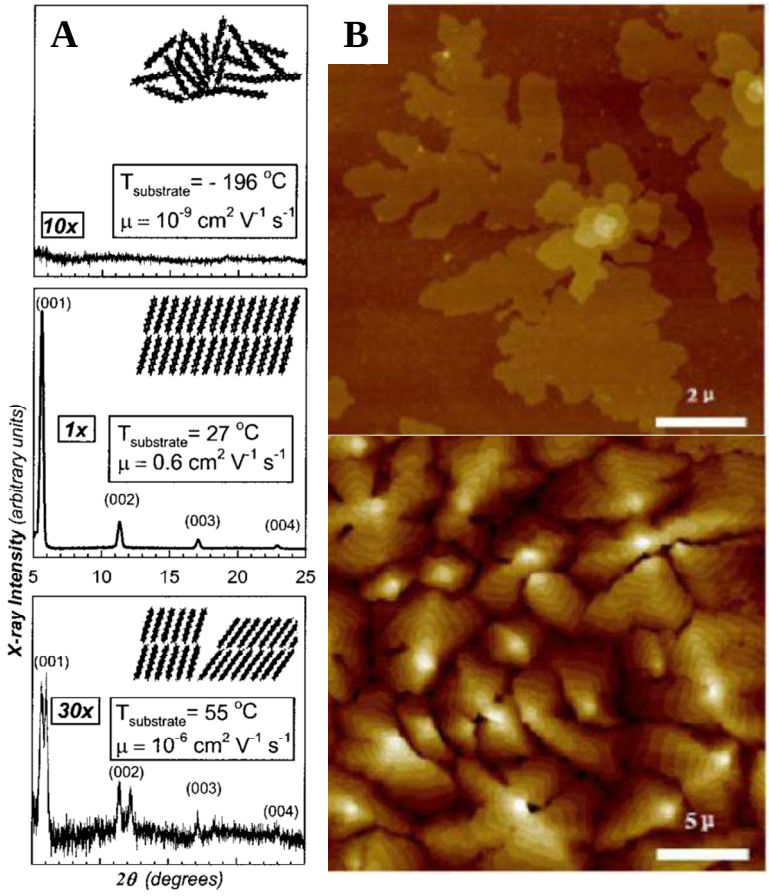

Figure 4.5 (A) X-ray diffractograms, schematic representations of structural order, and field-effect mobility corresponding to three different pentacene thin films deposited on SiO_2. Reproduced from (*1*). **(B)** AFM images of pentacene monolayers (top) and 10 nm thick film grown on SiO_2. Reproduced from (*12*).

In Figure 4.5A, we show X-ray diffractograms and field-effect mobility values for pentacene films evaporated onto oxidized silicon wafers held at three different temperatures. We see that for amorphous films created at low substrate temperatures (top) and high substrate temperature films with mixed phases (bottom), both the mobility and overall structural order are rather low. Room temperature deposition on

the other hand yields pentacene in mostly the *thin-film phase*, giving the most optimal conditions. For this structure, the long axis of the molecules stands nearly perpendicular to the substrate, giving a high degree of *p* orbital overlap. We note that this arrangement is qualitatively similar to the Herringbone configuration found in the bulk phase, although with a slightly different interplanar spacing (*4*). The importance and difficulty of good film synthesis is clearly evident here, as small changes in deposition parameters yield mobility values with orders of magnitude difference.

Even the most highly ordered films cannot be perfectly homogeneous, however. In Figure 4.5B, we show AFM images of both a few monolayers of pentacene (top panel) and for a thicker film (bottom) deposited on silicon oxide. We see that the first layer forms crystalline islands a few microns wide that are connected by grain boundaries. Grain boundaries are expected to adversely affect the electronic performance of the pentacene film, although we do not explicitly study their properties here. Subsequent island layers grown on top are progressively smaller, leading to a terraced morphology. From the point of view of device fabrication, however, the structure of these later layers is usually not as important in affecting electronic transport as we now discuss.

4.5 Fabrication of Pentacene Thin-Film Transistors

One of the greatest difficulties in fabricating devices from organic materials is that they are easily damaged in common solvents such as acetone. This makes them generally incompatible with the conventional lithographic process. For this reason, it is desirable to minimize the fabrication steps after the pentacene film is deposited, and

so using a degenerately doped silicon wafer as a global back gate is perhaps the most common gating method, as opposed to the fabrication of top gates, although that has also been demonstrated (*13*). If bottom gates are used, then most of the electrical conduction occurs in the first few deposited pentacene layers as they are more susceptible to the field effect. For this reason, the morphology of these monolayers is the most important in determining device performance. Having large grains of pentacene in the thin-film phase for the initial layers will yield higher device mobilities as we have already discussed.

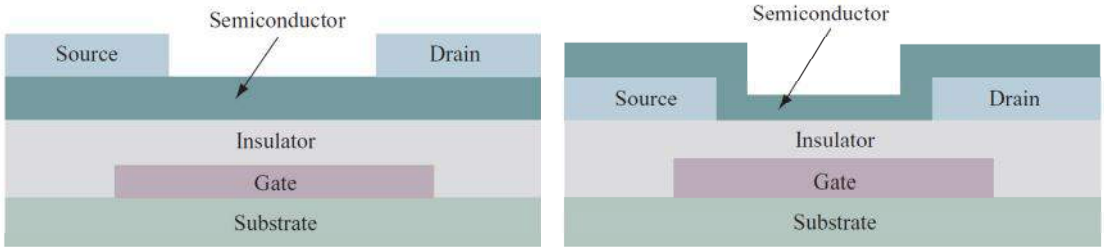

Figure 4.6 Schematic of top- and bottom-contact transistor geometries. Reproduced from (*14*).

There is another choice to be made as how to electrically contact the pentacene. We show two common device configurations in Figure 4.6. It is possible to put down electrodes after the film is deposited. This is called the *top-contact* geometry and is usually done with shadow masks. However, this method cannot be used in manufacturing, and so is considered to be not technologically applicable. Alternatively, one can define the contacts first using traditional lithography and deposit the film at the very end. This is called the *bottom-contact* geometry and is the

configuration we use for our devices. We shall see in the next section how the electrical performance of the two geometries generally differs.

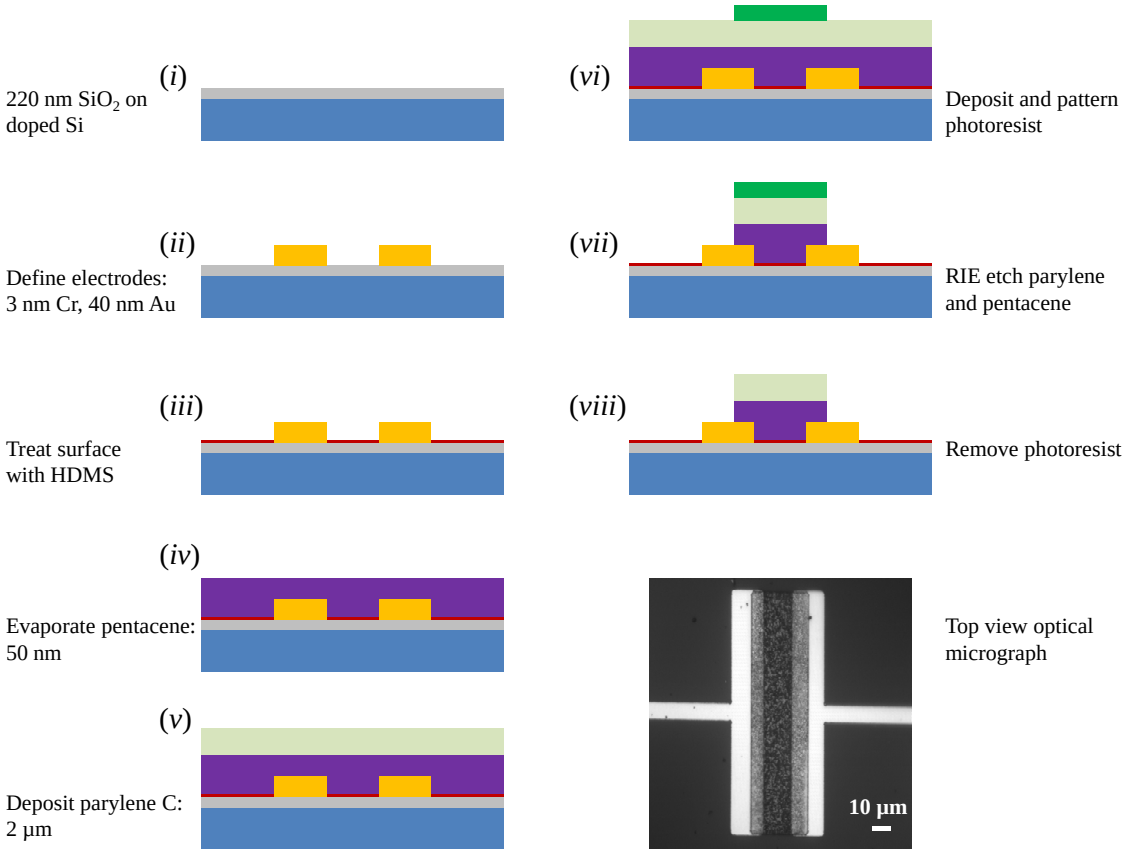

Figure 4.7 Step-by-step fabrication process for bottom-contact pentacene thin-film transistors used in this work. Optical image of finished device is shown in bottom right.

We now describe our specific fabrication procedure in greater detail. The process schematic is shown in Figure 4.7 along with an optical image of the finished device. We begin with a doped silicon wafer supporting 220 nm of thermally grown silicon oxide. Using optical lithography, we define source and drain electrodes (3 nm Cr/40 nm Au). We then passivate the wafer surface with hexamethyldisilazane (HMDS) before depositing 50 nm of pentacene by vacuum evaporation. In order to

localize the current flow in the channel between the source and drain electrodes, we next pattern the pentacene layer. However, since we must also prevent pentacene from direct exposure to solvents, we protect it with a 2 μm thick layer of parylene C. We then pattern conventional photoresist on top of the stack to use as an etch mask for the channel region. After the unprotected parylene and pentacene are etched away together by reactive ion etching (RIE), we remove the photoresist layer using acetone.

4.6 Summary

In this chapter, we covered a few introductory topics on the properties and fabrication of pentacene thin-film transistors that are needed to understand the current challenges facing their development. In the past, advances in film synthesis has led to dramatic improvements in pentacene device performance, making the material now competitive with amorphous silicon, which is used for large-area electronics applications. The key here has been the engineering of pentacene thin films with highly ordered structure. Naturally, we can ask whether there is room for further optimization and development. In the next chapter, we will show how the transport properties of the film body is not the only factor which determines overall electrical behavior. Efficient hole injection into the film from external metal electrodes continues to be a challenge for devices in the technologically more relevant bottom-contact geometry, as it is difficult to grow a continuous film across the interface.

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CHAPTER 5

IMAGING AND CHARACTERIZATION OF CHARGE INJECTION IN PENTACENE THIN-FILM TRANSISTORS

5.1 Introduction

The ongoing effort to improve the device performance of pentacene thin-film transistors has led to order of magnitude increases in field-effect mobility over the years (*1*). The series resistance that is attributed to charge injection from the contact is another aspect to the device optimization story. We have already mentioned that pentacene is a *p*-type semiconductor as the energy barrier for electron injection is too high. In turns out that efficient injection of holes into pentacene is also a challenging issue, and so has been the focus of intensive research. Intrinsically, there is a Schottky barrier of Φ_h = 0.5 eV for hole injection from gold. However, we shall see that the morphology of the film at the vicinity of the electrodes plays an even larger role in affecting the contact resistance of the device.

We start this chapter by reviewing previous work on the study of contact effects in pentacene thin-film transistors. We then proceed to discuss our own results using photoelectrical microscopy to image hole injection in pentacene. We observe that pentacene films only make pointlike contacts to the underlying gold electrodes, even for the best performing devices. Through a series of analyses, we determine that the resistance of each contact point is ≈1 GΩ. Furthermore, by optically nulling the resistance of just a single point, the overall device current can improve by ≈50%.

These findings of such surprisingly poor contact performance from gold would then motivate us to use graphene as electrodes for the pentacene film. Our preliminary results indeed show better morphological and photoelectrical behavior from this new device geometry. Much of this chapter is reproduced from (*2*).

5.2 Previous Work

There is already a substantial body of knowledge in the literature regarding contact effects in pentacene transistors. We discuss some well-known findings from a few representative works in this section.

Channel Scaling

Perhaps the simplest method to extract contact resistance is to fabricate and characterize devices of various lengths. A fit of the plot for resistance as a function of channel length will yield the value of contact resistance in the limit of zero length. In this manner, Necliudov *et al.* have studied both top- and bottom-contact pentacene transistors and determined that at gate biases where the device is turned on, the top-contact geometry shows significantly better contact resistance (Figure 5.1A) (*3*). This effect has been attributed to the different morphology of the pentacene film grown in the vicinity of the electrodes (*4*). In particular, the first pentacene monolayers grown on silicon oxide are large, highly ordered grains as we have seen. On the metal electrodes, however, the grains are much smaller and more disordered. This poor structure extends into the channel region, affecting charge injection into an otherwise higher quality film. The contrast in is clearly seen in the scanning electron microscopy

(SEM) images in Figure 5.1B, which shows the morphology of the pentacene film grown near and away from the electrodes. For top-contact devices, this issue is absent as the metallization occurs after film deposition.

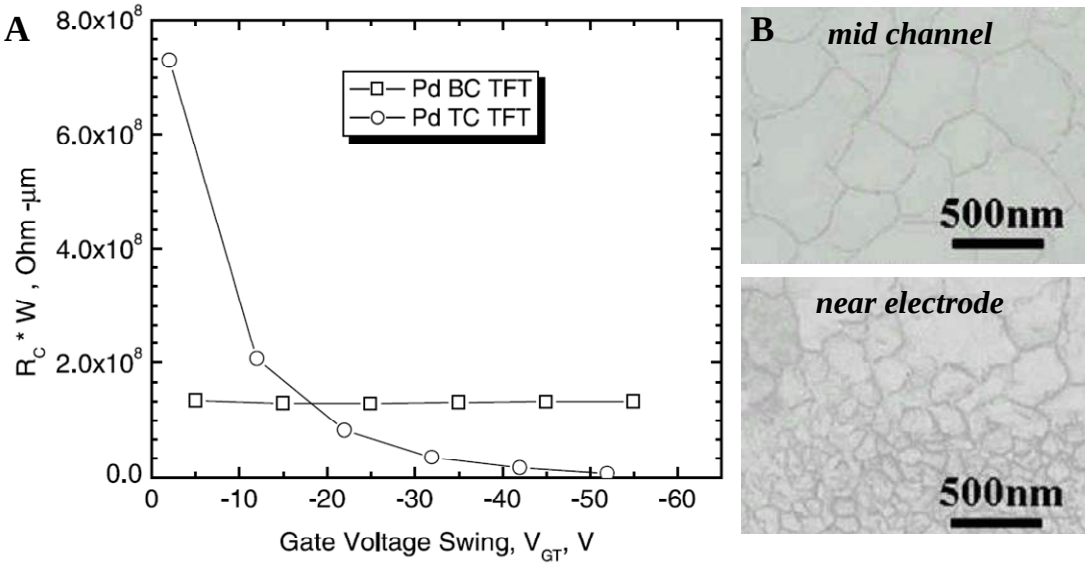

Figure 5.1 (A) Contact resistance in pentacene thin-film transistors for top (TC) and bottom (BC) contacted Pd electrodes extracted from channel scaling. Reproduced from (*3*). **(B)** SEM image of pentacene film in the middle of the channel (top) and in vicinity of Au electrodes. Adapted from (*5*).

Scanning Probe Measurements

While characterizing the length dependence of the channel affords a simple method to extract an average value for contact resistance across many devices, it does not provide information to distinguish individual devices, nor can it resolve variations in contact resistance along the width of the channel. For that purpose, one must be able to spatially image the effect of charge injection. Prior to our photoelectrical measurements, Kelvin force microscopy (KFM) had been used to image the surface potential across pentacene thin-film transistors. In Figure 5.2A, we show topography

and surface potential images for representative top- and bottom-contact devices from Puntambekar *et al.* (*6*). While the top-contact device shows a smooth change in surface potential along the length of the channel, the device with bottom contacts exhibits abrupt changes at both electrodes, indicating much larger values for contact resistance, consistent with previous results. This is seen more clearly in the line cuts shown in Figure 5.2B.

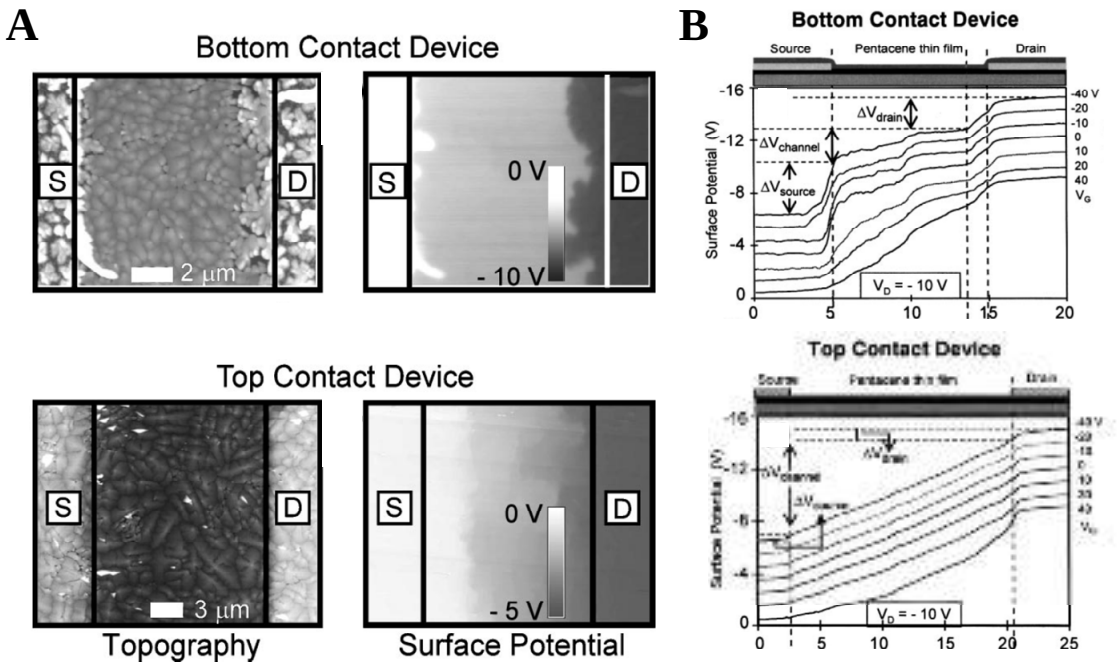

Figure 5.2 (A) Topography and KFM images of surface potential for bottom- and top-contact pentacene thin-film transistors. (B) Line profiles of surface potential. Reproduced from (*6*).

Scanning probe measurements, however, are most sensitive to the effects at the top of the pentacene film, whereas electrical transport mainly occurs in the bottom layers closer to the substrate. It is therefore important to understand the contact effects at the buried interfaces between the electrodes and initial pentacene monolayers. For

this, our scanning laser-based system can provide an ideal characterization platform, as both the pentacene film and parylene are transparent to visible light. For the remaining parts of this section, we shall discuss the results from our photoelectrical study of charge injection in bottom-contact pentacene transistors. The experimental setup is identical to that described in Section 3.3. Unless stated otherwise, we use λ = 658 nm and ≈100 μW laser excitation in our measurements.

5.3 Photoelectrical Imaging of Point Contacts

In Figure 4.4A, we showed representative *I-V* characteristics from our pentacene transistors. The field-effect mobility is ≈0.2 cm^2/Vs at saturation, on par to other state-of-the-art pentacene thin-film transistors. At low source-drain voltages, however, we observe nonlinear behavior, indicating the presence of an injection barrier.

Zero Bias Photocurrent Imaging

In Figure 5.3A, we show a photocurrent image of a representative device *P1* in false color for V_{DS} = 0 and V_{GS} = -20 V, with the grayscale reflection image overlaid for reference. While most of device is not electrically responsive to the effect of the laser, the current image exhibits striking spots of opposite polarity at the drain and source contacts. Zoomed in and separated reflection and current images of the boxed area at the drain (right insets) resolve the spots with greater clarity and reveal that they are located at the pentacene side of the interface, within the channel. The effect of contact photocurrent generation here is similar to that in carbon nanotube devices and

can be explained by the electronic band diagram shown in Figure 5.3B. While the band structure of the pentacene bulk is made strongly *p*-type by the action of the gate, the energy levels are pinned at the gold contacts, resulting in a potential gradient at the interface. Here, photogenerated carriers separate and induce a current when collected, with the sign dependent on the direction of band bending.

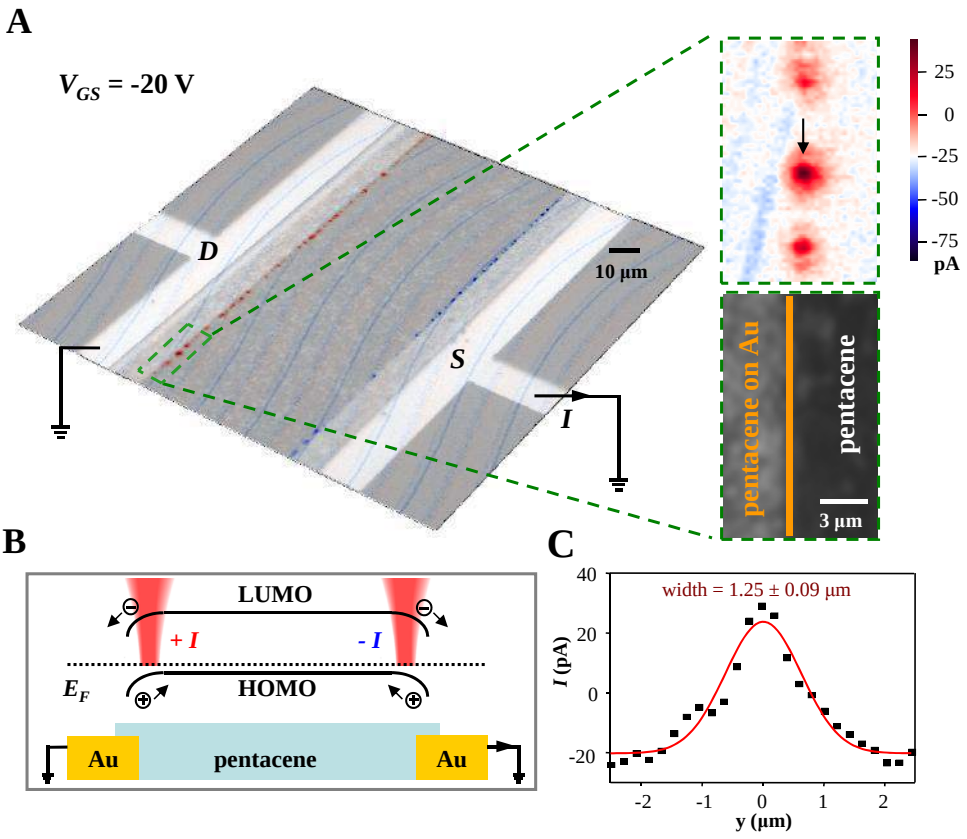

Figure 5.3 (A) Main panel: overlaid current and reflection (grayscale) images of device *P1* show spotlike current features of opposite polarity at source and drain contacts. Right: zoom-in of boxed area with current and reflection images separated. **(B)** Mechanism of photocurrent generation in pentacene induced by band bending at the contact. **(C)** Line cut of center photocurrent peak from above is fitted to a Gaussian with diffraction-limited width.

We have carried out measurements on over 50 pentacene devices, and all exhibit spotlike features of contact photocurrent. Furthermore, devices with a greater

number of photocurrent spots demonstrate better electrical performance overall. Substantiated by our measurements under bias to follow, this strongly suggests that these spots are the areas where the pentacene film makes good electrical contact to the gold electrodes, and hence, where hole injection occurs.

To further study the nature of the electrical contacts, in Figure 5.3C, a line cut of the central photocurrent spot in the zoomed in current image (marked by an arrow) is taken along the interface (vertical direction) and fitted to a Gaussian with width equal to that of the diffraction-limited laser spot. If pentacene formed extended contact to the electrodes, we would expect an elongated signal. Instead, we find that pentacene makes point contacts to the underlying gold within our resolution limits. This agrees with the morphology studies of Tsuruma *et al.* (*7*), in which the presence of localized physical contacts for the first few pentacene monolayers are attributed to the suppression of nucleation sites around the periphery of the gold. Therefore, despite the benefit of more continuous structure for the subsequent layers of pentacene growth, our results offer compelling evidence that hole injection occurs only at the localized contacts to the first pentacene layers for bottom-contact devices, although a close correlation with morphology would be necessary to explore this picture further.

Photoelectrical Imaging under Applied Bias

When a bias is applied across the device ($V_{DS} < 0$), a much different effect is observed. The main panel of Figure 5.4A shows the current image of *P1* for V_{DS} = -5 V and V_{GS} = -20 V. While the large background is due to dark current flow, now the most striking photoresponse is present only at the source electrode, an effect also seen

by Fiebig *et al.* in their biased pentacene device (*8*). When the laser illuminates certain areas along the hole injection contact, current levels nearly double from that of DC, with net photogenerated current $I_{ph} = I_{light} - I_{dark}$ two orders of magnitude larger than that at zero bias. A zoom-in of the boxed area is shown in the insets on the bottom for both $V_{DS} = 0$ and $V_{DS} = -1$ V. Comparison between the two images reveals that the same contact points at the source seen from zero bias photocurrent contribute to much larger photoenhanced signals under bias, suggesting that the laser assists in hole injection in the device (with electron injection being negligible at the drain).

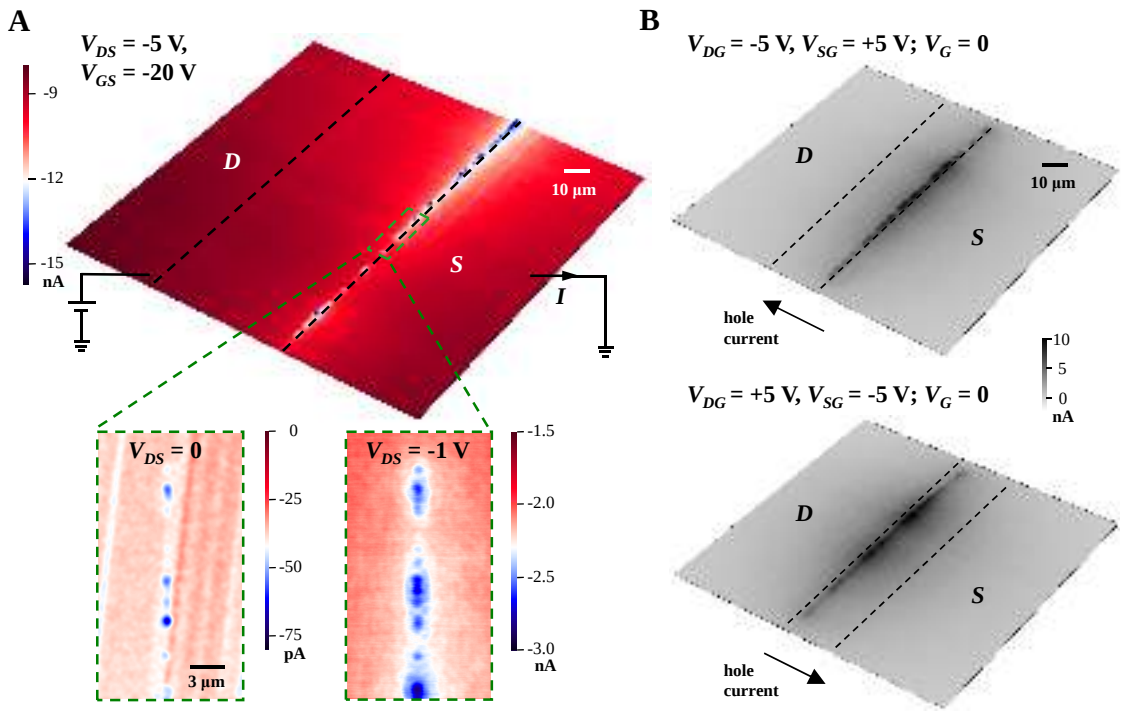

Figure 5.4 (A) Main panel: current image of *P1* for V_{DS} = -5 V, V_{GS} = -20 V. Bottom: zoom-in of boxed area for V_{DS} = 0 and V_{DS} = -1 V. **(B)** Magnitude of photogenerated current $|I_{ph}| = |I_{light} - I_{dark}|$ in device *P2* imaged under opposite bias conditions: V_{DG} = -5 V, V_{SG} = +5 V and V_{DG} = +5 V, V_{SG} = -5 V, with gate grounded.

We can corroborate this hypothesis by forcing hole injection at the opposite electrode. In Fig. 5.4B, we image $|I_{ph}|$ for device *P2* under opposite biasing conditions: V_{DG} = -5 V, V_{SG} = +5 V and V_{DG} = +5 V, V_{SG} = -5 V, with the gate grounded for both. For the former, we see the same effect as before: a significant rise in current levels when the laser strikes areas along the hole injecting source contact, with almost no features at the drain. However, the current features have shifted to the opposite contact for the latter, the side of hole injection under the new bias.

Photo-Assisted Hole Injection

We now try to understand the mechanism responsible for light-assisted hole injection in pentacene. The most direct way that light can enhance current in pentacene is via photoconductivity (*9-11*). While most photoelectrons generated in pentacene either recombine or fall into deep traps within a picosecond of excitation (*12*), a small fraction fall into shallow traps with a long lifetime before escape (*13*). These trapped electrons then attract additional holes from the source electrode, thus increasing current in the device (Figure 5.5A, top panel).

In particular, this trap-dominated photoconductivity mechanism is effective throughout our devices. In Figure 5.5B, we show the laser power dependence of I_{ph} when the laser is fixed at three locations on device *P3* for V_{DS} = -1 V, V_{GS} = 0: a contact spot at the source electrode (denoted by arrow, left inset) and two spots within the channel (midgap and close to the drain electrode). All data show good fits to a power law with subunity exponent (≈0.3 to 0.4), reflecting increased trap filling at higher light intensities (*11*). We have also measured the time response of current at the

source and midgap sites as an 11 mW laser is shuttered on and off (Figure 5.5C). Both show an initial fast rise and decay as the laser is shuttered (≈1 ms) as well as a slower component of ≈0.1 s, indicating the presence of at least two distinct electron trap states at both positions, consistent with previous reports (*10*).

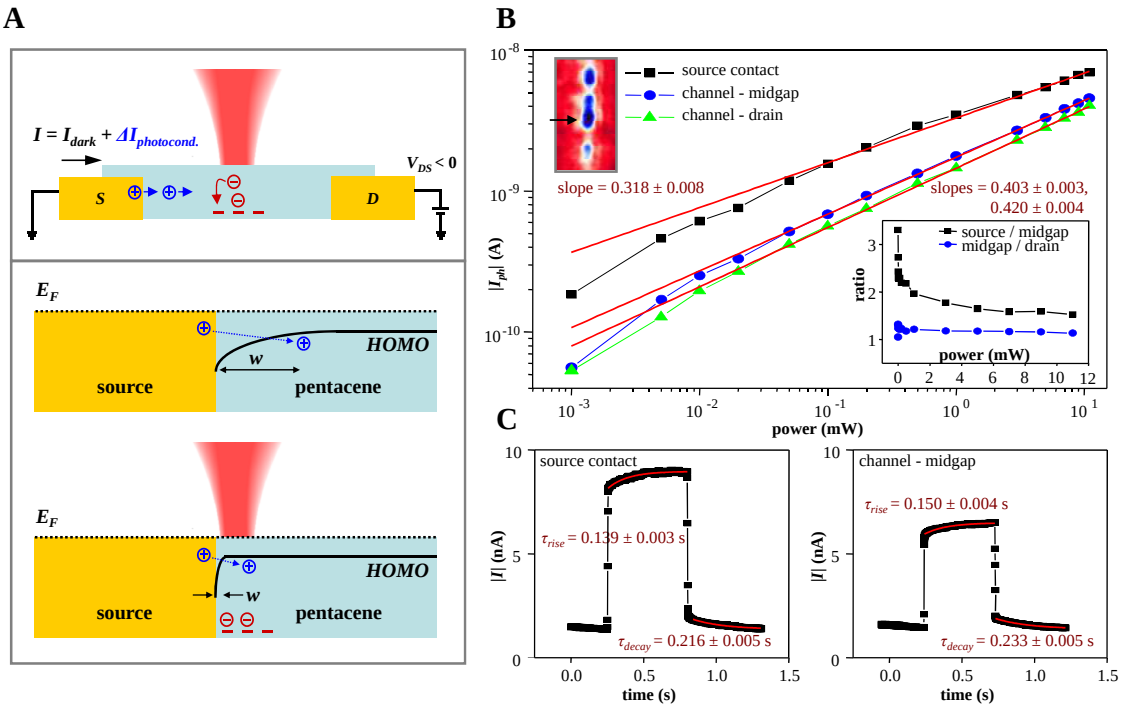

Figure 5.5 (A) Top: mechanism of photoconductivity in pentacene channel effected by electron trap states. Bottom: mechanism of light-induced reduction in interfacial resistance. **(B)** Main panel: power dependence of I_{ph} in *P3* for V_{DS} = -1 V, V_{GS} = 0 as laser is fixed at three positions on pentacene (contact at source: upper left inset, midgap in channel, and in channel close to drain). Bottom right inset: ratio of I_{ph} at different positions (source/midgap, midgap/drain). **(C)** Time response of current signals at source and channel midgap to 11 mW laser shuttered on and off.

Yet, photoconductivity alone cannot explain the pronouncedly enhanced photoresponse seen for the localized points at the source contact. In the inset of Figure 5.5B, we plot the ratio of I_{ph} measured at the source to that measured midgap in the channel as a function of laser power. I_{ph} at the source is especially dominant at lower

powers, decreasing relative to photoconductivity in the channel at higher powers. In contrast, the ratio of I_{ph} at midgap to I_{ph} close to the drain maintains a nearly constant ratio of ≈1.2 throughout the measured range. This suggests that a different mechanism unique to the hole injection contact is also at play.

To explain this source localized effect, we posit that the same electron trap states that contribute to photoconductivity, when situated at the injection electrode, will have an additional effect on the interfacial band structure. In particular, these negatively charged, immobile traps will locally dope the pentacene film at the contact, causing hole injection to become more favorable. As shown at the bottom of Figure 5.5A, whereas the energy levels in the pentacene bulk can be modified relative to the Fermi level by the action of the gate, they are fixed at the contacts by the metal electrodes. As a result, holes injected from gold to pentacene must overcome a depletion barrier region of width *w*. Previous scanning probe studies have revealed that this injection barrier translates to a large interfacial resistance R_i that can dominate the overall resistance of bottom-contact pentacene devices (*6*, *14*).

When the interface is under illumination, however, the same electron traps generated that induce photoconductivity will also act as *p*-dopants for the pentacene film by attracting additional holes to neutralize them. Their localized presence at the contact will, in effect, decrease the barrier width *w* and reduce R_i. This process is akin to the mechanism for lowering contact resistances in semiconductor devices, where increased dopant concentrations around the metal contact cause a reduction of the injection barrier (*9*).

Extraction of Point Contact Resistance

From our previous power dependence measurements at low source-drain bias (Figure 5.5B), we can estimate R_i at an individual hole injection point using the following circuit model (Figure 5.6A, left). The point contact under study is given a laser power, or trap density, dependent interfacial resistance $R_i(P)$, whereas the remaining nonilluminated contacts are lumped into a single resistor R_i' in parallel and the bulk channel resistance $R_{channel}$ is in series. When the laser of power P locally illuminates the source contact point measured in Figure 5.5B, we detect a change in current corresponding to the two distinct components of photoconductivity and increase in hole injection caused by reducing the interfacial resistance, $R_{i0} \rightarrow R_i(P)$:

$$I_{ph,source} = \Delta I_{photocond.} + \Delta I_i = \Delta I_{photocond.} + \left(\frac{V_{DS}}{R_{channel} + R_i(P) \,||\, R_i^{'}} - \frac{V_{DS}}{R_{channel} + R_{i0} \,||\, R_i^{'}} \right). \quad (5.1)$$

The injection component can be extracted experimentally from the total current change by subtracting the photoresponse midgap in the channel (where only photoconductivity is in effect).

In Figure 5.6A (right), we show $|\Delta I_i|$ as a function of laser power. At the lowest powers, $R_i(P)$ is large and close to the dark interfacial resistance R_{i0}, and so $|\Delta I_i|$ is small. However, $R_i(P)$ vanishes rapidly with increasing power until current saturates. A fit for the above expression for $\Delta I_i(P)$ yields $R_{i0} = 2.6 \pm 1.5$ GΩ for the point contact in Figure 5.5B, $R_{channel} = 354 \pm 3$ MΩ, and $R_i' = 415 \pm 3$ MΩ. We repeated the measurement for another contact on the same device and obtained similar resistance values.

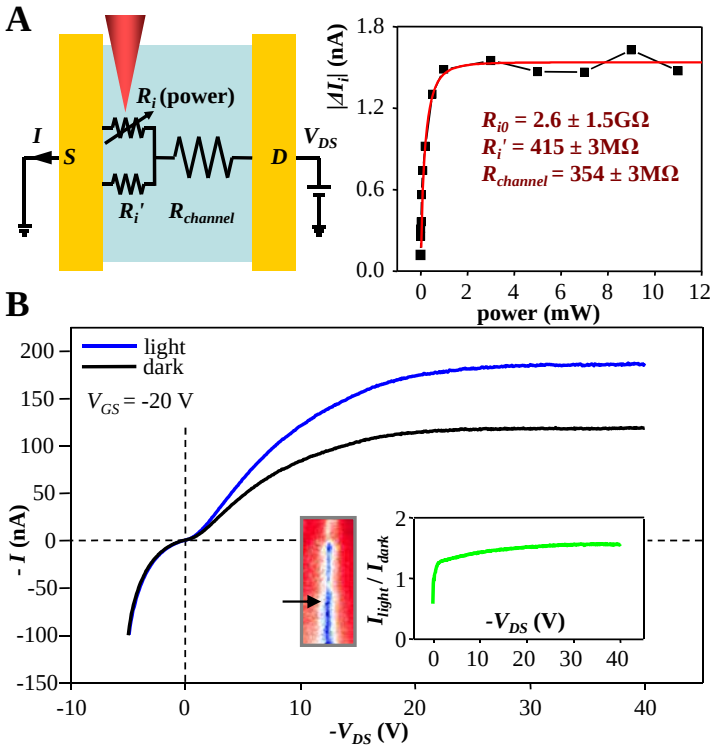

Figure 5.6 (A) Left: circuit model of interfacial resistance in pentacene device under study. Right: component of photogenerated current associated with reduction in R_i as function of laser power extrapolated by subtracting photoconductivity from the bulk and fit to the model described in the text. **(B)** Main panel: effect of reducing R_i at a single contact at source (bottom left inset) on device *P4* current characteristics for ≈100 μW laser. Bottom right inset: ratio of I_{light} to I_{dark} at same spot shows ≈50% current increase throughout $V_{DS} < 0$.

It is now clear that the point contacts play an important role in determining the properties of charge transport in pentacene transistors. As we have seen, focused illumination at a single hole injection site alone can increase current significantly even at relatively low light intensities due to a decrease in the interfacial resistance. To further demonstrate how this can improve the overall electrical properties of the device, in Figure 5.6B, we plot the output characteristics for device *P4* when the laser is focused on a particular contact at the source (marked with arrow in inset) for a moderate ≈100 μW illumination, where the injection component to photogenerated

current dominates, together with those of dark current. We see that the ratio of I_{light} to I_{dark} maintains a near constant ratio of 1.5 throughout almost the entire bias range (V_{DS} < 0), implying a ≈50% increase in device conductivity, and so, saturation current.

The collective results from our photoelectrical measurements thus lend naturally to the question of how charge injection can be improved in such systems. Since even our best performing devices with gold electrodes show pointlike contacts, perhaps the use of novel electrode materials may serve to reduce contact resistance, while still employing the more technologically relevant bottom-contact geometry. Previously, Kymissis *et al.* have demonstrated an overall improvement in the performance of bottom-contact pentacene devices when the gold contacts are treated with a self-assembled monolayer of 1-hexadecanethiol (*4*). The region of disordered film around the thiolated electrodes seems to disappear, forming a continuous morphology from contact to channel, although they do not explicitly determine the contact resistance from such devices. In the next section, we briefly describe some preliminary and alternative work characterizing the effect of using graphene electrodes for bottom-contact pentacene transistors.

5.4 The Use of Graphene Electrodes

Tsuruma *et al.* has shown that pentacene tends to avoid nucleation around gold electrodes (*7*). This could be caused by two distinct factors. First, as that work has pointed out, there is a large surface energy mismatch between the gold and silicon oxide, driving pentacene molecules onto the metal surface from the areas nearby, and so forming a denuded zone around the electrodes. Second, the physical height of the

metal contacts could also be a barrier to the formation of a more continuous film morphology. Anticipating that single-layer graphene could possibly mitigate both of these issues, we have fabricated bottom-contact pentacene transistors using graphene as electrodes. In Figure 5.7A, we show a schematic side view of the device geometry (top) along with an optical micrograph of a completed device just prior to evaporation of the pentacene (main panel). We will discuss the production of graphene in greater detail in the next chapter, but briefly, a continuous graphene film is grown on copper catalyst and then transferred to a degenerately doped and oxidized silicon wafer. After the graphene is patterned, gold electrodes are defined on top. The metal is recessed from the graphene edges, leaving a region of bare graphene to contact the pentacene film. Photoresist and a lift-off resist underlayer are then spun and patterned to form a window for the active area whereby evaporated pentacene can then be electrically isolated. The resists are then left on the device as their removal via solvents will also dissolve the pentacene film.

Unfortunately, the overall performance for these devices is rather poor: the average field-effect mobility is $\mu \approx 0.01$ cm^2/Vs. However, they do exhibit improved characteristics of charge injection. In Figure 5.7B, we show photoelectrical images of a representative device *PG1* for when $V_{DS} < 0$ and $V_{GS} < 0$. Here, instead of pointlike features at the contacts, we observe a more continuous line of photo-induced current at the negatively biased electrode, indicating more homogeneous hole injection along the channel width. This is further substantiated by examining the morphology of submonolayer film growth. In Figure 5.7C, we show SEM images of partially grown pentacene islands on silicon oxide near both gold and graphene electrodes. For the

former, pentacene islands tend to avoid crossing the interface, consistent with the findings of Tsuruma *et al.* (*7*). However, for the latter, we see many islands that have grown across the graphene contact and serving to actuate injection into the channel. These results suggest that graphene electrodes may provide a means to improve contact resistance in bottom-contact pentacene transistors, although other aspects affecting electrical transport clearly need to be optimized in order to confirm this.

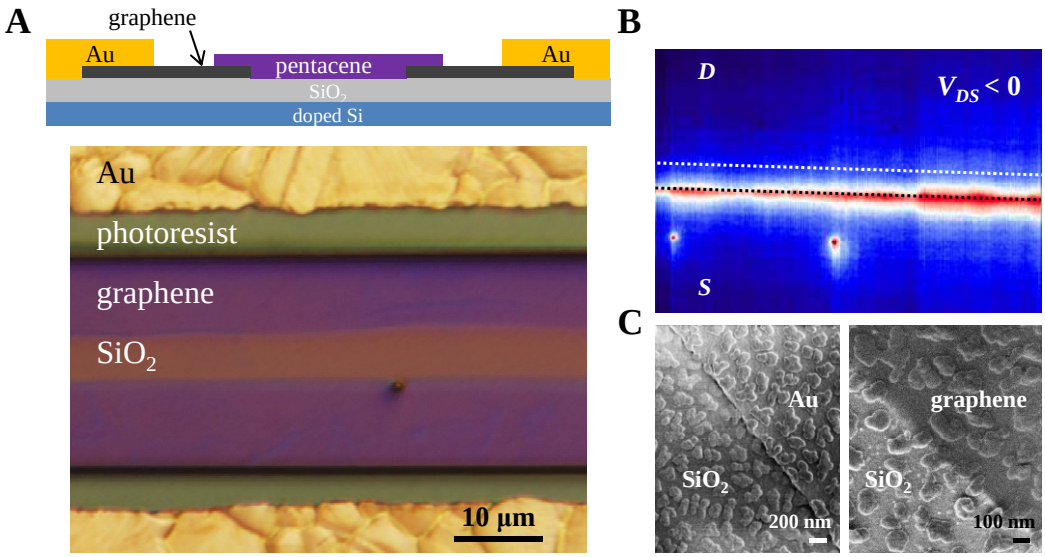

Figure 5.7 (A) Top: side view of pentacene transistor with bottom-contact graphene electrodes. Bottom: top view of device before pentacene evaporation. **(B)** Current image for device *PG1* for $V_{DS} < 0$, $V_{GS} < 0$. (C) SEM image of submonolayer pentacene growth around Au and graphene contacts.

5.5 Summary and Outlook

In this chapter, we reviewed some previous work studying charge injection and contact effects in pentacene, after which we presented our findings on the photoelectrical imaging and characterization of pentacene thin-film transistors, bottom contacted with gold electrodes. Zero bias photocurrent measurements revealed that

hole injection is localized to pointlike regions of contact, even for the best performing devices exhibiting state-of-the-art field-effect mobilities. From photoelectrical imaging under applied source-drain bias, we then determined the contact resistance for each point to be ≈1 GΩ. By improving the contact properties of just one of these points from laser illumination, we observed device current at saturation to increase by ≈50%. The results from our spatially resolved study clearly show that we are far from reaching the full potential in electronic performance from pentacene thin films. In the future, other novel electrode materials should be studied and characterized as well.

As a proof of principle, we have demonstrated a simple fabrication process for the use of graphene as bottom contacts to pentacene. While the overall electrical performance of the devices was rather poor, photoelectrical imaging revealed much more uniform contact features, motivating further trials and studies in the future. In addition, the thiol treatment of bottom gold electrodes for pentacene transistors has already led to improvements in overall device performance in the past. It would be interesting and worthwhile as well to image such devices using photoelectrical microscopy in order to characterize their contact properties with spatial resolution. Lastly, we need not only limit ourselves to the study of pentacene films, as the same experimental technique and methods can be used for the investigation of any conducting organic material.

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CHAPTER 6

THE GROWTH AND STRUCTURE OF POLYCRYSTALLINE GRAPHENE

6.1 Introduction

In this chapter, we discuss the structure of single-layer graphene, a truly two-dimensional material that possesses many remarkable electrical properties not found in other systems, such as ultrahigh carrier mobility and linear electronic band structure. These discoveries were only recently made possible by isolating small graphene crystals from bulk graphite via a process called *mechanical exfoliation*. In order to exploit graphene for technological applications, however, one must be able to synthesize large-area graphene films with uniform characteristics. Recently, the science of graphene has experienced revolutionary change, mainly due to the development of several large-scale growth methods. In particular, graphene synthesis by chemical vapor deposition (CVD) on copper has provided an especially reliable method for obtaining such films with mostly monolayer coverage. At the same time, these graphene films are polycrystalline, consisting of multiple graphene crystals joined by grain boundaries. These defect structures in an otherwise homogeneous lattice could potentially alter the electrical behavior of the film as they are predicted to possess distinct electronic properties. However, understanding their precise effects on transport locally is nontrivial as one must first possess the capability to accurately image them.

As we have already derived the electronic structure of graphene in Section 2.2 in discussion of single-walled carbon nanotubes, we begin the chapter by describing the two main graphene production methods mentioned above in greater detail. We then discuss the structure of large-area graphene films synthesized by CVD. In particular, we will show how *dark field transmission electron microscopy* can be used to image grains and grain boundaries in these films on a large scale. These techniques and studies will pave the way for our measurements on the electrical properties of individual grain boundaries in the next chapter. Parts of this chapter are reproduced from (*1*) and (*2*).

6.2 Production of Graphene

There actually exist several different methods to produce graphene sheets on vastly different size scales, but here, we shall only discuss two in detail: that of mechanical exfoliation from graphite, producing small flakes of the highest quality, and large-area synthesis via CVD. While the first measurements on graphene were made from exfoliated samples, the method is unfeasible for large-scale electronic applications. The CVD synthesis of graphene solves this problem, but at a cost to the material's structural homogeneity.

Mechanical Exfoliation

While the concept of single-layer graphene has been understood for a long time (the name being coined in 1962 in discussion of bulk graphite (*3*)), the material was not isolated until late 2004 (*4*). The exact procedure first used by the Manchester

group is rather complicated and has developed into several variations over time. Nonetheless, the principle rests on the realization that the individual graphene layers in highly oriented pyrolytic graphite are loosely bound to each other via Van der Waals interactions. Using ordinary scotch tape, one can then repeatedly peel off thin layers and stick them onto arbitrary substrates, such as oxidized silicon wafers (Figure 6.1). The thickness of these flakes can then be identified optically (*5*), making it relatively easy to electrically address few or single layers of graphene using electron beam lithography for device measurements.

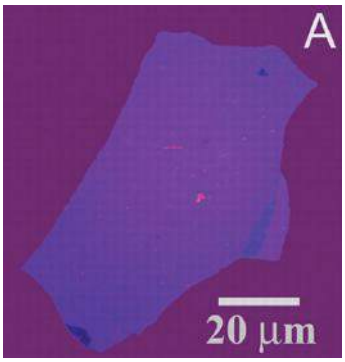

Figure 6.1 Optical micrograph of exfoliated multilayer graphene flake on SiO_2/Si wafer. Reproduced from (*4*).

Chemical Vapor Deposition

If graphene is to be integrated into relevant technological applications, however, simple mechanical exfoliation cannot possibly satisfy the size and scale requirements for such efforts. Recently, graphene synthesis by CVD on copper has emerged as one of the most convenient techniques to obtain high-quality, single-layer graphene. A schematic of the growth process is shown in Figure 6.2A. Briefly, the copper substrate is heated to ≈1000 °C in a low pressure CVD chamber under a

reducing environment to remove its native oxide. Methane gas is then flown. It decomposes on the surface of the copper which acts as a catalyst for the largely self-limiting growth of single-layer graphene. In the next section, we shall discuss how the flow rates of the gases as well as the length of the growth period affect the structure of the graphene film. After the growth, graphene can then be transferred to arbitrary substrates using a simple copper etching process (*6, 7*). Over time, the CVD method has been developed and scaled to produce graphene films on even the meter length scale (*8*).

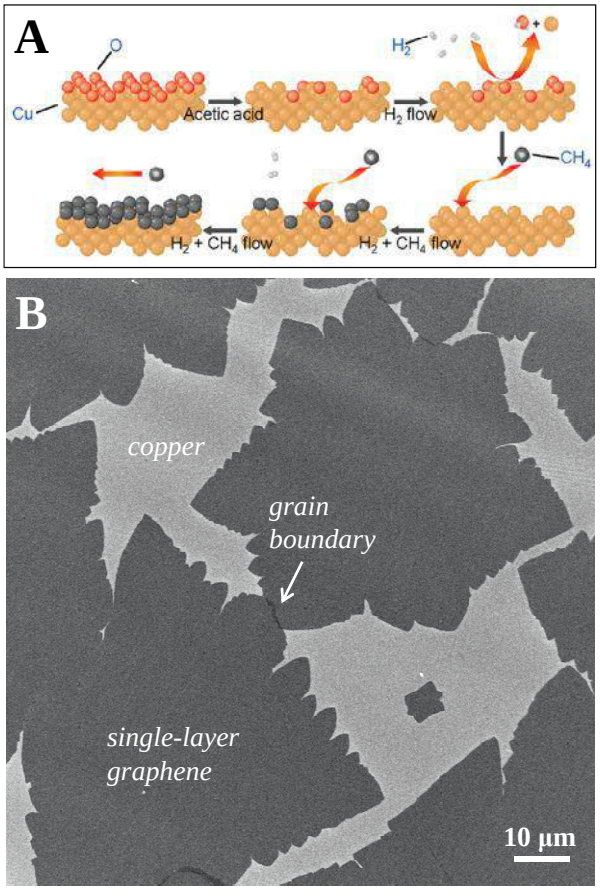

Figure 6.2 (A) Schematic of CVD graphene growth on copper. **(B)** SEM image of partially grown graphene islands on copper foil.

When materials are assembled in macroscopic sizes, however, their homogeneity becomes an important issue. For the case of CVD grown graphene, this can be clearly understood from Figure 6.2B, which shows a scanning electron microscopy (SEM) image of graphene which had grown to only partially cover the underlying copper surface. We see that graphene has nucleated at multiple sites and grown to form discrete island structures. Since each island may consist of a distinct crystal orientation (or *grain*) that is rotated with respect to that of its neighbors, their intersections will form defect structures known as *grain boundaries*. The presence of grain boundaries in an otherwise uniform graphene film could potentially alter their behavior, as theoretically, they are predicted to have a unique electronic structure deviating from that of the pristine graphene lattice (*9*). The electrical properties of grain boundaries will be the subject of careful discussion in the next chapter. First, however, we require a microscopy tool that can image the crystalline structure of graphene, so that we can precisely identify individual grains and grain boundaries in the CVD film.

6.3 Transmission Electron Microscopy of Grains and Grain Boundaries in Polycrystalline Graphene

Many microscopy techniques have been applied to provide spatially resolved information about the structure of graphene. Both transmission electron microscopy (TEM) and scanning tunneling microscopy have demonstrated the ability to provide unrivaled atomic scale images of the graphene lattice, for instance (*10-12*). However, such high resolution microscopy techniques are usually slow and would require

prohibitively long acquisition times to image a sample even on the micron scale. In this section, we shall introduce an alternative imaging technique, also based on TEM, which can be used to map the different grain orientations in CVD graphene over large areas with high-throughput. We then use it to characterize graphene synthesized under different growth conditions. Finally, we discuss how the structure of grain boundaries may also grow differently depending on these conditions.

Dark Field Imaging of Grain Structure

In standard, *bright field* TEM imaging, contrast is observed when different regions of the sample show different levels of transparency to the principal electron beam. However, many transmission electron microscopes also possess the capability to image in a configuration that is specifically sensitive to electron diffraction. This imaging mode is called *dark field* TEM (DFTEM), the mechanism of which can be understood from the top panels of Figure 6.3. In Figure 6.3A, Huang *et al.* shows a typical bright field TEM image of CVD graphene fully suspended on top of a hole, which exhibits almost no contrast difference across the sheet (*10*).

The electron diffraction pattern from this area, however, shows many sets of sixfold symmetric spots (Figure 6.3B). Since a single crystal of graphene would yield one such set of diffracted spots due to the lattice symmetry, this diffraction pattern implies that the area contains many distinct graphene crystals. In order to image this area in dark field mode, one can place a small aperture in the diffraction plane to collect only the electrons passing through it (denoted by the while circle in Figure 6.3B), thereby selectively imaging the graphene grains diffracting in this small range

of angles (Figure 6.3C). By repeating this process with several different aperture positions (Figure 6.3D), one can colorize and then overlay all the dark field images to generate complete maps of the grain structure in this area (Figure 6.3E). Here, we see many grains emerge from a common center, which could indicate that it is the location of a nucleation site.

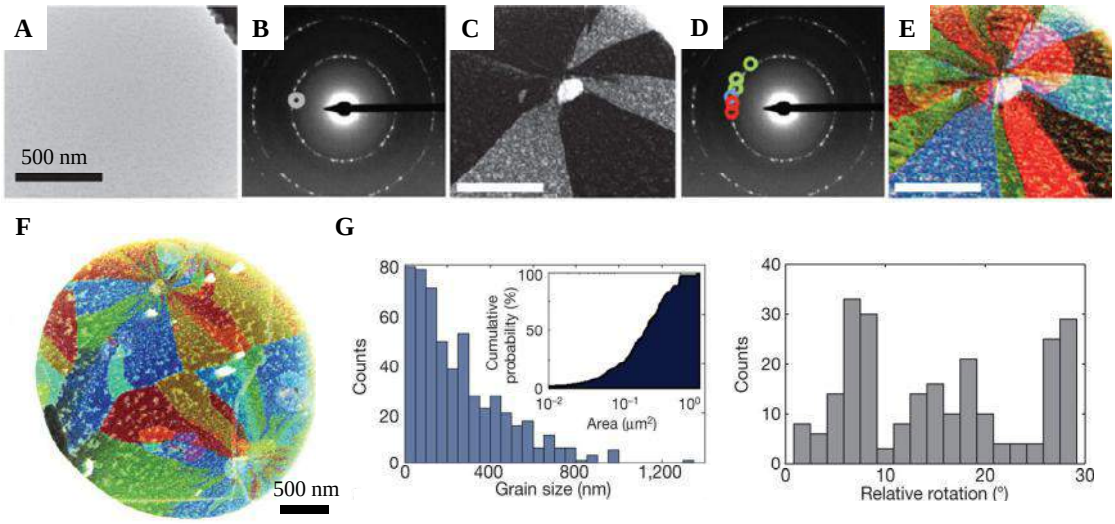

Figure 6.3 (A-E) DFTEM process for characterization of graphene grain structure. **(F)** Color coded, large-scale image of grains in graphene film. **(G)** Histograms of grain size (left) and relative rotation between grains (right).

By performing DFTEM over larger graphene areas, as in Figure 6.3F, one may quickly obtain statistical distributions for the sizes of individual grains as well as the relative rotation angles between the lattices of neighboring grains (Figure 6.3G). For this particular sample, the mean grain size is only ≈250 nm; however, this will depend strongly on the synthesis conditions. We also observe a preference for both low and high angle grain boundaries.

Grain Size and Synthesis

Over the years, many groups have developed variations in CVD synthesis to obtain graphene films with different physical morphologies (*7*, *13*, *14*). Following these established growth procedures, we have studied the grain structure of the resulting films using DFTEM, and we shall discuss the findings for three such growths, denoted as *A*, *B* and *C*.

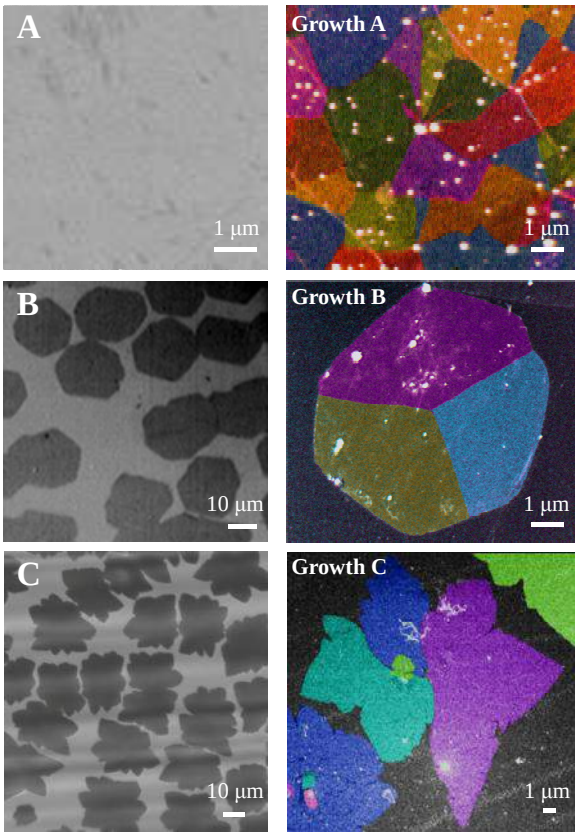

Figure 6.4 (A) SEM (left) and DFTEM images of growth *A* graphene. **(B, C)** Optical (left) and DFTEM images of growth *B* and *C* graphene.

In growth *A*, graphene has been synthesized under relatively high reactant flow rates (CH_4: 6 sccm, H_2: 100 sccm), which produce a fast growth to uniformly cover

the entire copper surface (Figure 6.4A). However, we see from DFTEM that it also creates a high density of sites where graphene growth nucleates, and therefore, the average grain size $D \approx 1$ μm is relatively small. Graphene from growth *B* has been synthesized in a diluted methane environment (CH_4: 0.8 sccm, H_2: 300 sccm), while the copper for growth *C* was put in an enclosure to further reduce its exposure to the reactants (CH_4: 1sccm, H_2: 60-120 sccm). This suppresses the nucleation density of graphene, which leads to larger grain sizes. Growth *B* yields $D \approx 10$ μm and growth *C* produces $D \approx 50$ μm in continuous films. These results clearly show that while the CVD growth of graphene is a robust process, the morphology of the film is keenly sensitive to growth conditions, as it is possible to tune the average grain size by nearly three orders of magnitude via only small changes to the reaction environment.

Finally, decreasing nucleation density also leads to slower growth times for both growths *B* and *C*, and so their films shown in Figures 6.4B and 6.4C have been terminated after only partial surface coverage to highlight their growth structures. We see that the overall shapes of partially grown graphene islands in growth *B* are polygons, while growth *C* generally forms flowered islands. Despite these seemingly simple growth structures, DFTEM shows that even a single graphene island can contain several distinct domains within it, further revealing the complexity of the growth process.

The Structure of Grain Boundaries

The findings presented in the previous sections demonstrate unequivocally that CVD growth produces polycrystalline graphene films, with the average size of

graphene grains tunable during synthesis. We now turn to the study of the most prominent defects in CVD graphene: grain boundaries. It is also natural to ask whether their structure also depends on growth conditions.

Despite the absence of atomic resolution, it is still possible to use DFTEM to study the morphology of individual grain boundaries. Figure 6.5A (left) shows a DFTEM image of a grain boundary from growth *A*. The diffraction spots corresponding to each grain are circled with their respective colors in the inset. On the right, both spots are selected simultaneously with the aperture, and the resulting dark field image shows a seamless boundary. This suggests that the grain boundary forms an abrupt junction whose finer features cannot be resolved using DFTEM. High resolution TEM imaging, however, can provide images of the graphene lattice with atomic detail. Figure 6.5B shows a micrograph of a particular grain boundary from this type of growth taken with an aberration-corrected scanning transmission electron microscope by Huang *et al*. (*10*). Here, we see that the two grains are connected by an aperiodic arrangement of pentagons, heptagons, and distorted hexagon defects. A similar structure has also been seen by Kim *et al*. on their samples as well (*11*).

The growth that produces the largest grains, on the other hand, does not exhibit a tendency to form atomically abrupt intergrain connections. In Figure 6.5C, we show two grains from growth *C* that have physically connected. However, simultaneously selecting the diffraction spots for both domain orientations reveal a dark strip 30 nm wide where the grains join. This result implies that this extended boundary region has a different structure than the crystals on either side, suggesting that the domains are either joined together by graphitic material at another orientation or by amorphous

material. In fact, the presence of grain boundaries with greater crystalline discontinuity appears to be a general trend for growth *C*.

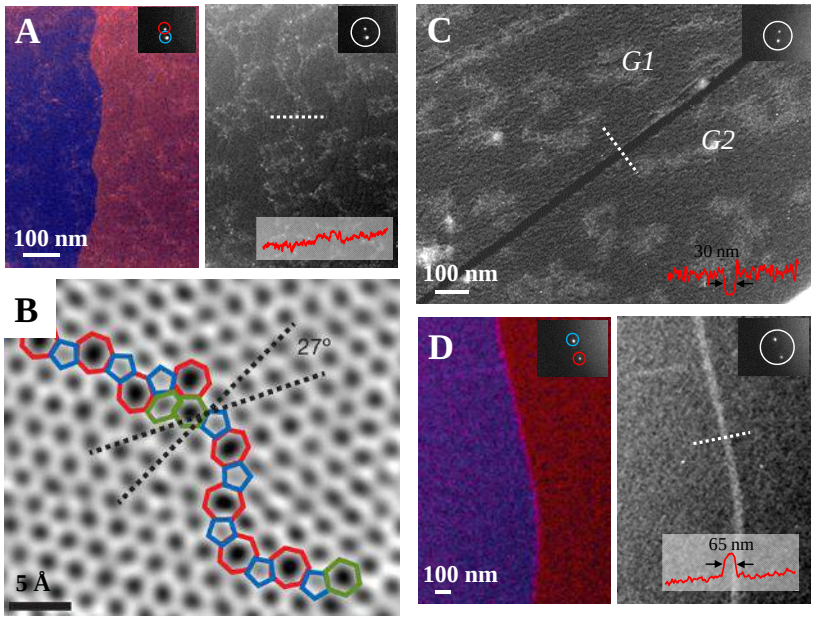

Figure 6.5 (A) Main panels: DFTEM images of a growth *A* grain boundary. Inset: diffraction spots and apertures used to generate image. **(B)** High-resolution TEM image of growth *A* grain boundary. **(C)** DFTEM image of growth *C* grain boundary. **(D)** DFTEM image of overlapped grain boundary from growth *C*.

Additionally, we observe grains in growth *C* to connect via an overlapping region. An example is shown in Figure 6.5D. Again, the overlap is seen most clearly by selecting diffraction spots from both grains simultaneously, as the double layered region appears twice as intense in the dark field image. Here, one domain extends 65 nm on top of the other, although overlaps as large as 1 μm are observed for longer growths. Similar behavior has also been observed by Robertson *et al.* using atomically resolved TEM imaging (*15*). We therefore conclude that the structure of grain boundaries in CVD graphene are not universal, but are rather sensitive to growth

conditions and reflect the quality of the connection between grains. In particular, the higher reactivity environment from growth *A* which yields a faster growth rate and smaller grain size could also contribute to better grain stitching.

6.4 Summary

We began this chapter by discussing two common ways to produce graphene. The initial discoveries of graphene's properties were made possible by its mechanical exfoliation from bulk graphite, a time-consuming process giving low-throughput. More recently, it has been made feasible to synthesize graphene films on a large scale using CVD. By using DFTEM to image their diffraction patterns, we found that these films are polycrystalline and consist of many distinct crystal grains stitched together by grain boundary defects. Furthermore, both the average grain size and grain boundary structures are highly dependent on synthesis conditions. These structural differences will be clearly manifested in their electrical properties as we shall see in the next chapter.

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CHAPTER 7

ELECTRICAL PROPERTIES OF GRAIN BOUNDARIES IN POLYCRYSTALLINE GRAPHENE

7.1 Introduction

Since grain boundaries are defects in an otherwise periodic lattice, they are expected to enhance the scattering of carriers in their vicinity, and therefore, decrease the overall electrical performance of the material. The degree of scattering would naturally reflect the precise structure of the grain boundary. It is then necessary to understand the separate electronic effects of the different grain boundary types we have observed in graphene grown by chemical vapor deposition (CVD), as this could be a key step in the optimization of their synthesis. Addressing this important issue will be the focus of this chapter.

In principle, one may electrically address an individual grain boundary once its structure has been clearly identified and characterized by transmission electron microscopy (TEM). In practice, however, complicated sample preparation processes and constraints arising from chip geometry have previously made TEM studies largely incompatible with other experimental schemes such as nanofabrication. Here, we describe a novel process combining dark field TEM (DFTEM) imaging with electrical measurements. It allows us to study transport across individual grain boundaries together with an understanding of their structure. We also discuss the implications of our results for the performance of large-scale polycrystalline devices. For

completeness, we begin by introducing the intrinsic electrical transport characteristics of single-crystal graphene, as prepared by mechanical exfoliation. We also review prior experimental work characterizing the electronic properties of grain boundaries in CVD graphene. Much of this chapter has been reproduced from (*1*).

7.2 Electrical Conductance in Single-Crystal Graphene

Even though graphene does not possess a band gap, it is still possible to modify its conductivity via electric gating. In the limit of zero temperature, intrinsic graphene is, in principle, an insulator, since no electronic states exist at the Dirac points. Unfortunately, such ideal conditions are never realized, not only due to the effects of finite temperature, but also because the position of the Dirac point cannot be perfectly uniform across the entire sample. Realistically, graphene possesses a finite, minimum conductivity (*2*). Away from the Dirac point, graphene's conductivity is expected to increase as the electronic density of states for both electrons and holes increases with carrier density.

Indeed, such behavior is universally observed in graphene field-effect transistors. In the main panel of Figure 7.1A, we show gate dependent conductivity plots taken from five devices fabricated using mechanically exfoliated graphene. The curves are vertically displaced for clarity. An optical micrograph of one representative device is shown in the inset. At the Dirac points, σ takes on the lowest value. Away, σ increases monotonically with increasing gate voltage of either polarity. We notice that the rate of increase in conductivity is similar for both electron and hole doping, reflecting the ambipolar symmetry of carriers in graphene. Alternatively, one may also

plot resistivity ρ or sheet resistance (resistance normalized to device dimensions) $R_{\square}$ = ρ = 1/σ, which will simply show the inverse behavior.

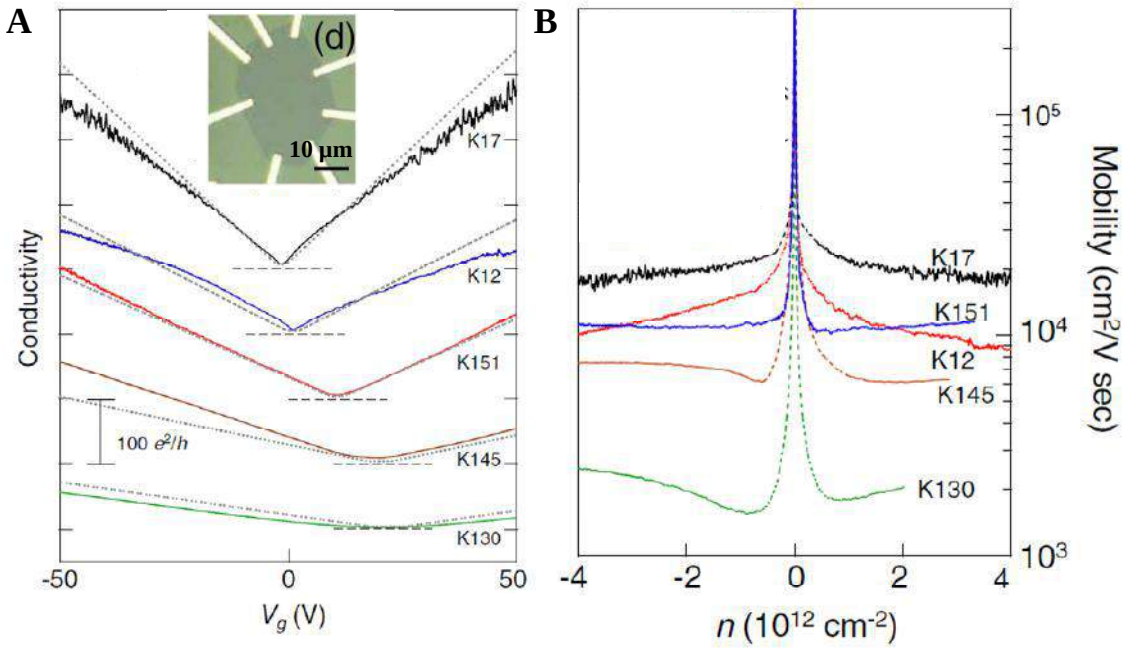

Figure 7.1 (A) Inset: optical image of representative graphene transistor device. Main panel: gate dependent conductivity for five different graphene devices. Curves are vertically offset. **(B)** Mobility as a function of carrier density extracted from Drude model. Adapted from (*2*).

An important metric to gauge the performance of graphene devices is the carrier mobility μ, which can be extracted in two ways. First, one can determine μ from the Drude model directly, as $\mu = \frac{\sigma}{en(V_G)}$, where $n(V_G)$ is the gate dependent carrier density. We show μ calculated this way for the same five devices in Figure 7.2B. Alternatively, one can measure field-effect mobility from the slope $d\sigma/dV_G$ just as in ordinary semiconductors. Both methods, however, are not valid too close to the Dirac point, as μ diverges for the former and approaches zero for the latter in the limit of zero n. Slightly away from the Dirac point, mechanically exfoliated graphene

exhibits $\mu_{electron} \approx \mu_{hole} \approx 10^3$ to 10^4 cm^2/Vs for devices on silicon oxide, and up to $\approx 10^5$ cm^2/Vs for suspended devices (*3*), making it one the highest performing electronic materials measured to date.

7.3 Previous Work

Intuitively, due to the presence of grain boundary defects, CVD graphene films are expected to exhibit inferior electronic performance than single-crystal graphene prepared by mechanical exfoliation. Theoretically, however, it has been predicted that electrical transport across graphene grain boundaries with perfectly periodic structures may be either highly transmissive or reflective over a wide range of energies, simply depending on the relative orientations of adjacent domains (*4*). One such extended defect structure has been experimentally identified using scanning tunneling microscopy (STM) on graphene grown on nickel and its electronic density of states spectrum revealed metallic character, in contrast to the semimetallic properties of the graphene sheet (Figure 7.2A) (*5*). As shown in the previous chapter, however, grain boundaries in CVD graphene may not form periodic defect structures even on the nanometer scale. It is therefore important to understand the impact of realistic graphene grain boundaries on electrical transport.

In the work of Huang *et al.*, electrostatic force microscopy (EFM) measurements were performed on polycrystalline CVD films to spatially map the surface potential across the device (*6*). Within instrument limits, they did not detect any sharp changes in potential that would be caused by increased resistance from grain boundaries, and so concluded that grain boundaries in graphene are very conductive

(resistance less than 60 Ω per μm length) (Figure 7.2B). In contrast, Yu *et al.* and Jauregui *et al.* synthesized graphene islands in the shape of polygons and inferred the locations of grain boundaries from islands that have merged (*7*, *8*). Their electrical measurements on these structures found that interisland transport was indeed more resistive than that within an island, which they attributed to additional scattering caused by the grain boundary (Figure 7.1C). Their data extracted from six devices showed a spread of grain boundary resistivity from 60 to 2000 Ω-μm.

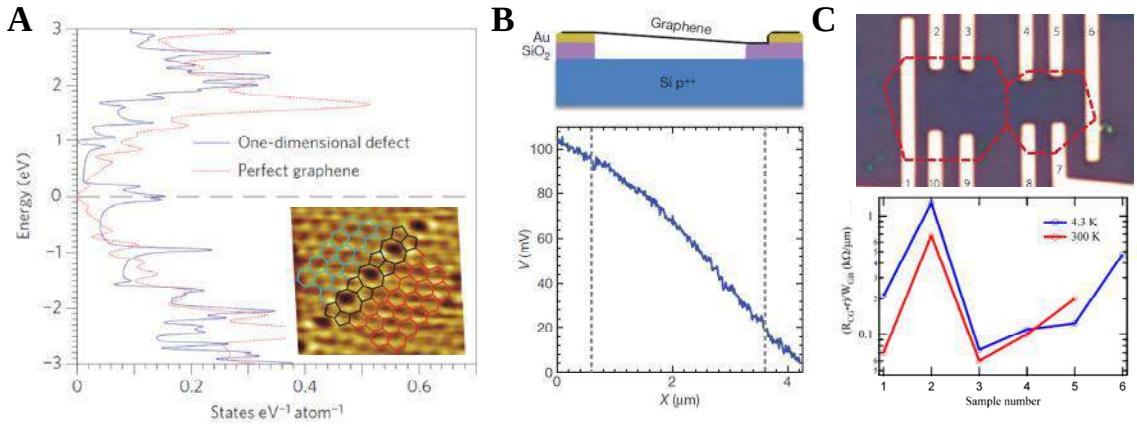

Figure 7.2 (A) Inset: STM image of extended defect in graphene. Main panel: electronic density of states spectrum of defect and pristine graphene. Reproduced from (*5*). **(B)** Bottom: line profile of surface potential in a suspended polycrystalline graphene device probed by EFM. Top: device schematic. Reproduced from (*6*). **(C)** Top: electrical device on two merged graphene islands. Reproduced from (*7*). Bottom: distribution of grain boundary resistance. Reproduced from (*8*).

The conclusions from these separate experiments may seem contradictory. However, at this point, it is difficult to clearly interpret their results because the grain morphology of the graphene devices under study is unknown, and so we do not have knowledge of the precise locations and structures of the grain boundaries. This is especially problematic in light of our previous DFTEM findings, which show that

even single graphene islands may often be polycrystalline. Furthermore, the precise carrier dopings for these devices are not well-defined, and as we shall see in the coming sections, the grain boundary resistance is not a constant, but instead can be modulated by a gate field.

7.4 Combined Platform for Microscopy and Electrical Characterization

In order to address these issues, we have developed a novel experimental process combining DFTEM with field-effect transport measurements. In Figure 7.3A, we show optical images of a specially fabricated TEM chip that is 2.33 mm wide on each side, 200 μm thick, and fits standard TEM holders. In the center is a fully suspended silicon nitride (SiN) TEM window (80x80 μm, 20 nm thickness) that is transparent to the electron beam. We have patterned small alignment marks in the central area as well as large electrical leads and contacts on the periphery. After graphene is transferred and imaged with DFTEM, we can then select an area of interest to pattern a field-effect transistor device.

These chips are fabricated on the wafer scale using optical lithography and cleaved individually at the end. The process flow is diagrammed in Figure 7.3B. First, we grow 50 nm of low stress SiN on 200 μm thick <100> silicon wafers. In two separate lithography steps, we pattern and metalize alignment marks and electrical leads close to the TEM window (20 nm Cr/Au) as well as contact pads on the chip periphery (150 nm Cr/Au). Next, we pattern and etch large windows in the SiN on the back side of the chip using reactive ion etching (RIE) to allow for potassium hydroxide (KOH) etching of the silicon substrate underlying the TEM window. After

transferring graphene, the TEM window is further thinned from the back to ≈20 nm with RIE.

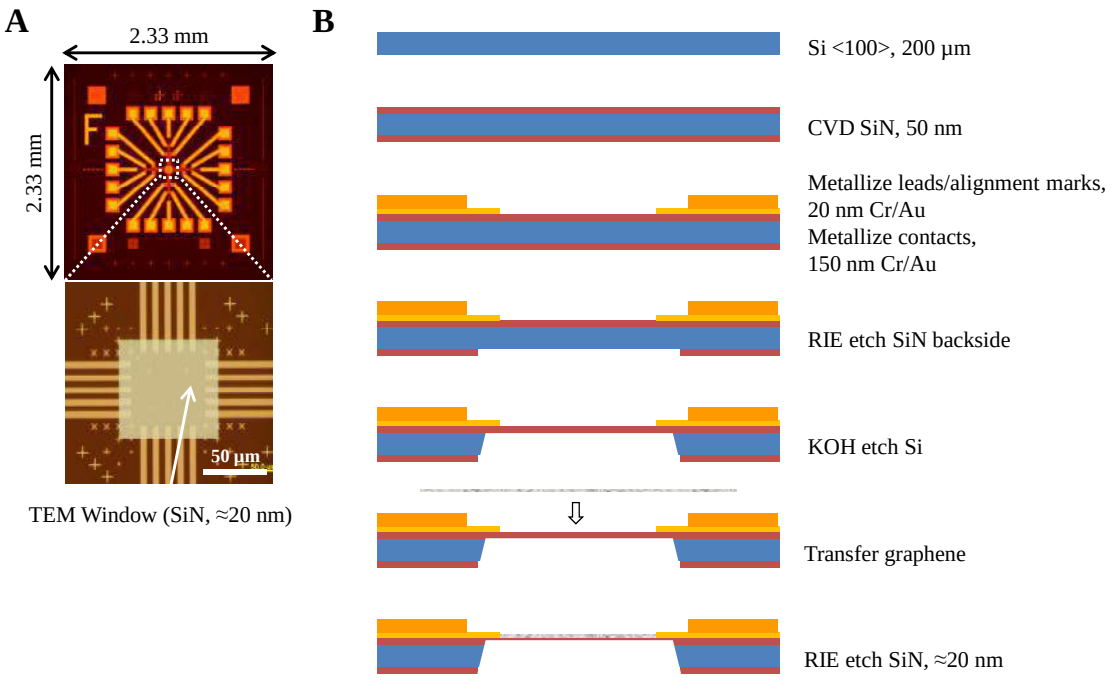

Figure 7.3 (A) Top: optical image of specially fabricated TEM chip. Bottom: zoom in of TEM window. **(B)** Step-by-step fabrication process.

After DFTEM characterization, we use three separate electron beam lithography steps to: (i) define electrodes; (ii) patterned the graphene; and (iii) define a top gate. A completed structure is shown in the SEM image in Figure 7.4A. The devices are designed in a Hall bar geometry in order to allow for four-terminal electrical measurements: current is passed between the end leads, while voltage is measured at the fingers in the middle in order to measure the resistivity of graphene separate from that of the metal leads and contacts. In Figure 7.3B, we show a scanning electron microscopy (SEM) image of a representative device (before defining the top gate) overlaid with the DFTEM image of the underlying graphene consisting of a

single grain boundary between two large grains from growth *C*. The areas with faded colors represent graphene that was subsequently etched away, leaving behind only the high contrast pattern in the center. In general, we are able to address features observed in TEM with ≈50 nm accuracy.

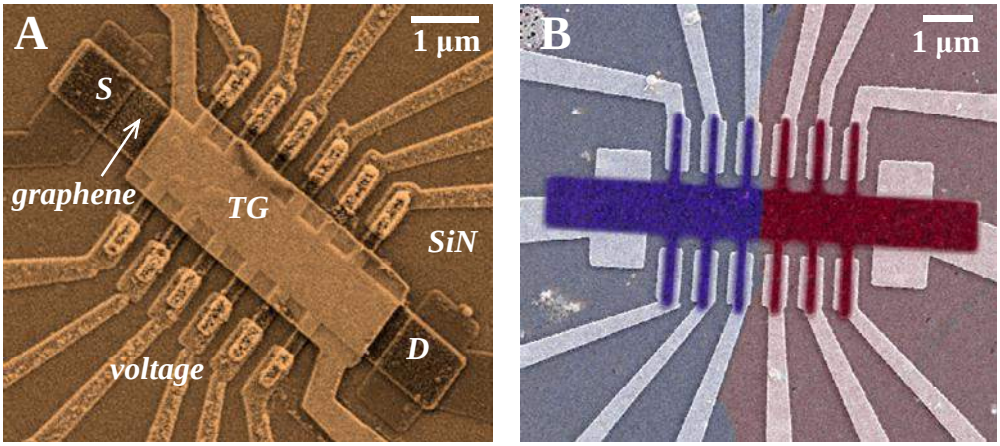

Figure 7.4 (A) SEM image of graphene device fabricated on SiN membrane. **(B)** Overlaid DFTEM and SEM images of device consisting of single grain boundary before defining top gate.

7.5 Electrical Measurements of Individual Grain Boundaries

We first performed transport measurements on a grain boundary from growth *A* (*D* ≈ 1 μm). In the inset of Figure 7.5A, we show the composite image of the device. In the top panel, we plot four-terminal sheet resistance $R_{\square}$ vs. gate voltage for the left (L) and right (R) domains, as well as that across the grain boundary (L-R), measured simultaneously for the same gate voltage sweep. The single grain measurements show field-effect behavior that is typical for graphene with a Dirac point at $V_{Dirac} \approx 7$ V. More strikingly, the two show nearly identical values for the entire gated range. The cross grain measurement shows qualitatively similar behavior with a comparable

Dirac position. However, L-R exhibits an increased resistance, particularly at gate biases near V_{Dirac} that we attribute to additional scattering caused by the grain boundary. Also, the resistivity of L-R seems to scale from single grain resistivity ($\rho_{\square}$) by a constant factor of 1.4 for all gate values, as shown by the dashed curve. Finally, by subtracting the averaged L and R values from L-R, we can extract the resistivity per micron length of the grain boundary itself, ρ_{GB}, which we plot in the bottom panel as function of gate voltage. ρ_{GB} exhibits a similar gate tunable behavior as $\rho_{\square}$: it is 4 kΩ-μm at V_{Dirac} and decreases with doping, reaching a saturated value of 0.5 kΩ-μm in the *p*-type regime.

The results of our measurement can be interpreted to describe the presence of a grain boundary as being simply an extension of the conductance channel by an effective length $\lambda = \rho_{GB}/\rho_{\square}$. When a device of dimensions L and W crosses a grain boundary, resistance increases from the intrinsic, monocrystalline resistance $R = \rho_{\square}(L/W)$ to $R' = \rho_{\square}(L/W) + \rho_{GB}/W = \rho_{\square}(L+\lambda)/W$. Hence, the channel length effectively increases by λ, and both the electrical conductance and carrier mobility are reduced by a factor $R'/R = 1+ \lambda/L$. Because R'/R closely follows a fixed scaling with gate voltage in our measurements, λ is approximately constant and independent of carrier density. This effect is diagrammed in the inset. The introduction and determination of λ, along with average domain size D, will allow for the tailoring of electrical transport in devices of all length scales as we shall discuss in the next section. For this particular device, we extract $\lambda \approx 200$ nm.

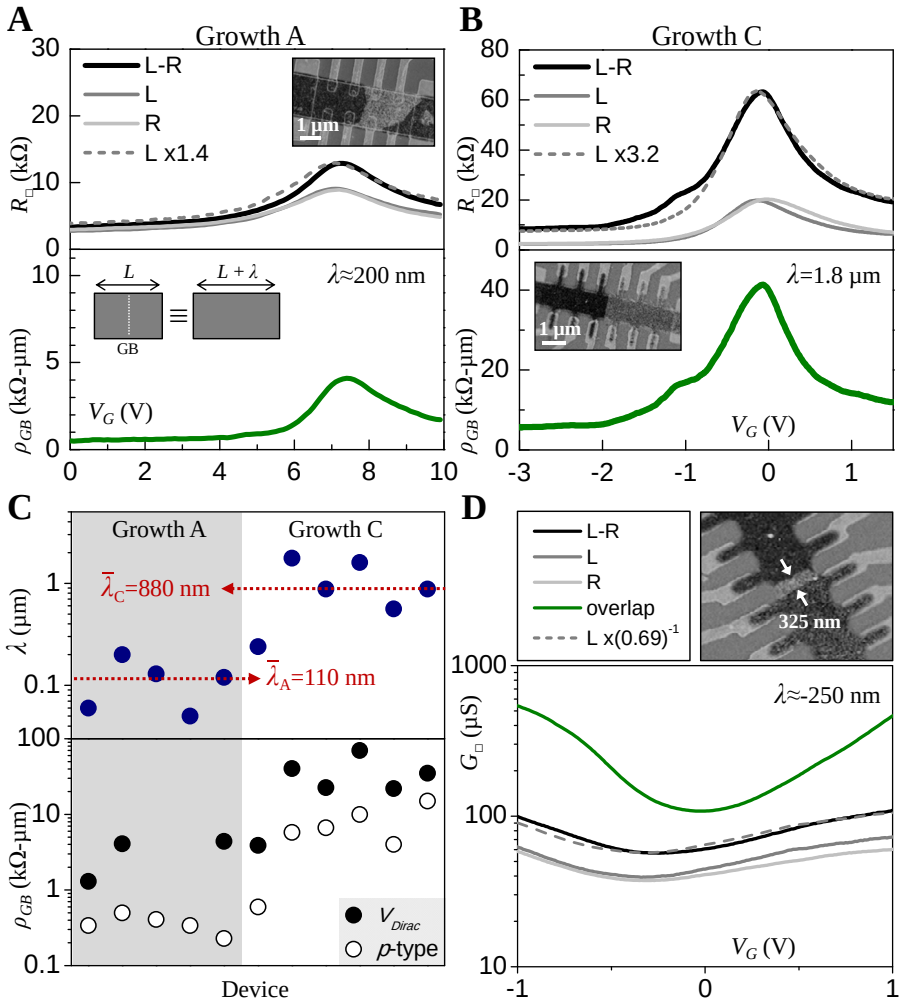

Figure 7.5 (A) Top panel: four-terminal sheet resistance $R_\square$ of device crossing a single grain boundary from growth *A* (SEM/DFTEM shown in inset) measured in left (L), right (R), and across (L-R) domains as function of gate bias. Bottom panel: extracted gate dependent grain boundary resistivity ρ_{GB}. Grain boundary acts to increase channel length by $\lambda \approx 200$ nm. **(B)** Corresponding measurement of more resistive grain boundary from growth *C* device: $\lambda = 1.8$ μm. **(C)** λ and ρ_{GB} (at V_{Dirac} and *p*-type doping) across 11 single grain boundary devices from growths *A* and *C*. **(D)** Electrical measurements of device consisting of grain boundary overlapped by 325 nm show improved conductance: $\lambda \approx -250$ nm.

Different electrical behavior is observed for analogous measurements at a grain boundary from growth *C* ($D \approx 50$ μm), which we show in Figure 7.5B. Here, L and R also show similar gate dependences, but L-R is considerably greater at all gate values, signifying increased scattering at the grain boundary. In fact, we extract a gate

dependent grain boundary resistivity (5 to 40 kΩ-μm) that is overall an order of magnitude greater than that measured for growth *A*. Nevertheless, $R'/R \approx 3.2$ is again roughly constant with gate bias, from which we determine λ = 1.8 μm for this grain boundary, or twice as long than the device channel itself.

We have fabricated 11 graphene devices with a single grain boundary and performed similar measurements (five devices from growth *A* and six from *C*). In Figure 7.5C, we plot their grain boundary resistivities measured both at V_{Dirac} and when *p*-type. Even though we observe a range of different values, grain boundaries from growth *C* are an order of magnitude more resistive overall. We also plot the corresponding gate independent λ values. The mean for growth *A* samples is $\bar{\lambda}_A$ = 110 nm, while $\bar{\lambda}_C$ = 880 nm for growth *C*. The interpretation of these results is clear given our observations from the previous chapter. The electrical properties of grain boundaries are also not universal, but rather reflect the structural quality of intergrain stitching. In particular, the better connected grain boundaries from growth *A* exhibit much smaller resistivities and λ values overall.

We have also fabricated a device across two grains from growth *C* that have overlapped at their boundary, which we show in Figure 7.5D. Here, the grains overlap by 325 nm. Instead of an increased cross grain resistance, we observe that conductance $G_{\square} = 1/ R_{\square}$ is enhanced by a factor of 1.45, which implies an effective negative $\lambda \approx$ -250 nm. We also plot the square conductance from the overlapped graphene exclusively by removing contributions from the L and R grains, and we see that it is an order of magnitude greater than that for single-layer graphene. This then suggests that the scattering properties in double-layer graphene are improved from that of only one

layer, although further studies are required to verify this. Nevertheless, our finding motivates the reliable synthesis of grain boundaries with large overlap, as electrically, they could prove to be the most optimal grain boundaries in polycrystalline films. At this time, however, their formation is still largely uncontrolled.

7.6 Large-Area Electronics with Polycrystalline Graphene

The results discussed in the previous section suggest that it is necessary to control grain boundary connectivity as well as domain size in order to maximize the overall electrical transport properties in polycrystalline graphene films. For this, it is essential to develop a systematic understanding of the combined electrical effect of λ (representing grain boundary connectivity) and D (domain size) under various graphene growth conditions and device geometries. Below, we present a simple model based on these two empirically derived parameters that can be used to optimize electrical performance in graphene devices at all length scales.

There are two necessary criteria to uphold in order to successfully integrate CVD graphene into electronic applications. Not only is it important to maximize the performance of individual graphene devices, but achieving uniform performance across many devices is also highly desirable. Because grain boundaries introduce inhomogeneity in the graphene film on the length scale D, a tradeoff occurs for the above two criteria. In the limit where device size $L = W << D$, graphene consisting of a single grain will clearly have the best individual performance, as device resistance is $R = \rho_{\square}$. However, devices that cross a grain boundary will have $R = \rho_{\square}(1+\lambda/L)$, which could pose a hindrance if λ is large, such as in growth *C*. In the opposite limit where L

>> D, the devices see $R = \rho_{\square}(1+n\lambda/L)$, where n is the number of grain boundaries crossed. However, we expect $n \approx L/D$, and so all devices will see a uniform $R \approx \rho_{\square}(1+\lambda/D)$, which also may not severely degrade performance if λ is small, such as in growth *A*. The plot in Figure 7.6A captures what is described here quantitatively. Here, we calculate normalized device resistance $R/\rho_{\square}$ as a function of device size L up to 15 μm for graphene from the two electrically characterized growths *A* ($D \approx 1$ μm) and *C* ($D \approx 50$ μm). The curve in black shows the result of growth *C* crossing one grain boundary using the empirically obtained $\bar{\lambda}_C = 880$ nm. Normalized resistance is very large at small L and decreases asymptotically to 1, the intrinsic limit without grain boundaries. The curve in blue shows the result of growth *A* as the device crosses the expected number of grain boundaries $n = L/D - 1$ (the error bars indicate a $\pm\sqrt{n}$ standard deviation from this number, rounded to the nearest integer). Here, resistance is 1 at small L and slowly increases, as calculated by $\bar{\lambda}_A = 110$ nm. The two curves cross at $L \approx 9$ μm. However, even above this length the growth *A* sample will not significantly degrade in performance as resistance eventually saturates to only 10% ($\approx\lambda/D$) larger than the intrinsic limit for single crystal graphene. Similarly, device mobility will approach 90% ($\approx 1-\lambda/D$) of that of a single crystal. Of equal importance, such devices show uniform performance over a large range of lengths with less likelihood of failure for an individual device.

This analysis suggests that well stitched grain boundaries are not the dominant scattering mechanism to affect large-scale device transport and points to an exciting potential for the high electrical performance of polycrystalline graphene. While the

synthesis of growth *C* could, in principle, be further optimized to achieve large grains together with better grain boundary connectivity, it seems we can already achieve most of the performance capability of single-crystal graphene in large scale, polycrystalline devices using our current growth conditions (growth *A*), despite limited grain size.

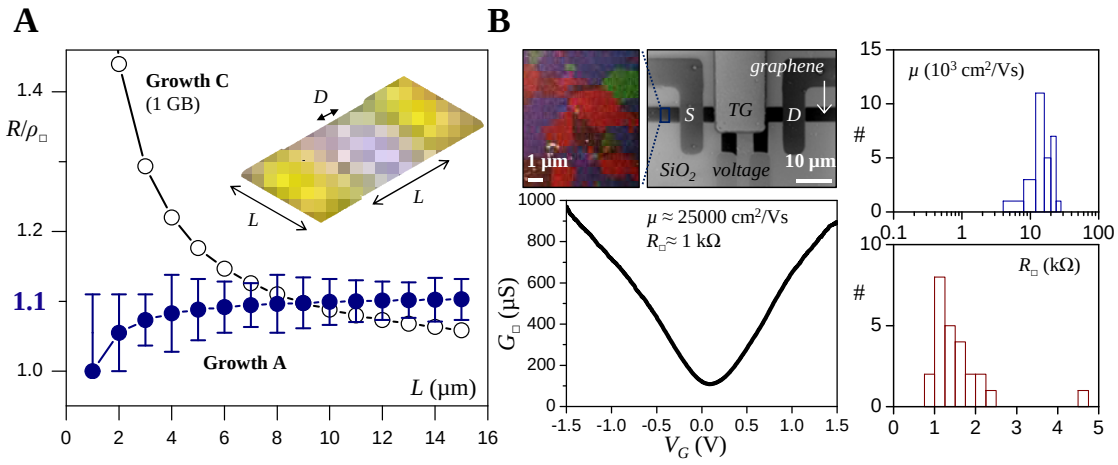

Figure 7.6 (A) Model of device resistance as function of device size for growth *A* and *C* using empirically determined λ and *D*. **(B)** Left: grayscale SEM image of ≈5x5 μm growth *A* type graphene device fabricated on SiO_2/Si and representative color DFTEM image of grain structure. Transport characteristics demonstrate performance on par with exfoliated graphene. Right: Histograms for field-effect mobility and *p*-type sheet resistance of 28 similarly fabricated devices show excellent electrical behavior overall.

We now demonstrate the performance potential of such samples experimentally, as shown in Figure 7.6B. We have fabricated a set of ultraclean graphene devices (≈5x5 μm) on oxidized silicon wafers using growth *A* type synthesis and conventional lithography without the additional imaging steps of TEM. For a particular high-performance device, we achieve a field-effect mobility of 25000 cm^2/Vs and sheet resistance of ≈1 kΩ at a relatively low carrier density (≈3×10^{11} cm^{-2}) (Figure 7.6B top), on par with that of mechanically exfoliated graphene (*2*). On the

right, we plot statistics across 28 similarly fabricated devices, and observe that almost all devices have field-effect mobilities above 10000 cm^2/Vs and resistances below 2 kΩ. Hence, grain boundaries in CVD grown, polycrystalline graphene can indeed be optimized to have a minimal electrical impact on the overall transport properties of the device, in accordance with our model and findings above.

7.7 Summary and Outlook

In this chapter, we discussed a novel experimental scheme to combine TEM with electrical measurements in order to study the effects of electronic transport across individual grain boundaries. We found that all grain boundaries behave to extend the conduction channel by an effective length λ, however, this length is very sensitive to the quality of stitching produced during synthesis. For better connected grains $\lambda \approx 100$ nm, while $\lambda \approx 1$ μm for grain boundaries with poor stitching. The most ideal grain boundary may actually be one where the two grains are largely overlapped as it is possible to obtain a negative λ value for such a structure. Unfortunately, their synthesis is yet mostly uncontrolled.

The results of these findings have very important ramifications for electrical transport in larger scale devices involving polycrystalline graphene films, geometries that are more likely to be used in technology applications. We have shown that it is important to control both grain size and intergrain connectivity in order to optimize for total device performance. In fact, we were able to demonstrate exceptional performance from smaller grain graphene films with better grain boundary

connectivity that is on par with that of exfoliated samples, further paving the way for use of CVD graphene in electronics applications.

Finally, our experimental scheme is completely general and can be used to characterize any nanomaterial. Lately, research on graphene has inspired a growing interest in the study of other two-dimensional electronic materials, such as molybdenum disulfide (*9*), a semiconductor, and bismuth telluride (*10*), a topological insulator. We anticipate that polycrystallinity and grain boundaries will be important reoccurring issues when these materials are grown in large areas.

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CHAPTER 8

CONCLUSION

8.1 Thesis Summary

In this thesis, we have used two different experimental techniques to study electrical transport in three different nanomaterials with spatial resolution, an important objective given their reduced dimensionality. Using photoelectrical microscopy, which combines a scanning, focused laser beam with electrical measurements, we were able to directly image the electrical conductance of individual carbon nanotubes *in situ*. The underlying mechanism here is the photothermal effect, in which laser absorption by the nanotube causes a change in its conductance. In general, the measured conductance change is proportional to the overall conductance of the nanotube itself, allowing for a local probe of its electrical properties via the focused laser. In a different mode of operation, we were also able to image internal electric fields in carbon nanotubes resulting from the bending of their electronic bands. This effect is most pronounced at the electrode contacts, where band pinning by the metal may lead to the presence of significant fields at either the exact interface or slightly within the nanotube body due to the formation of *p*-*n* junctions in semiconducting nanotubes. Furthermore, both of these imaging modes can be extended to characterize many carbon nanotubes simultaneously in large-scale device geometries.

We have also studied the electrical properties of pentacene thin films using photoelectrical microscopy. Here, the strongest signal is also seen at the interfaces to the bottom contacted gold electrodes. Surprisingly, however, the photocurrent features are always spotlike, rather than being homogenously distributed along the width of the channel. This led to our finding that pentacene films only make point contacts to the underlying gold. Devices with a larger density of contacted points also exhibit better electrical performance overall. Through a series of measurements and their analysis, we were then able to determine that the resistance of each point is ≈1 GΩ. The cause for such poor contact features can be attributed to the energy difference between the metal and silicon oxide surfaces, which acts to repel the nucleation and growth of pentacene at the interface. In order to tackle this issue, we were then motivated to use graphene as bottom electrodes for the pentacene film. While, the overall performance of such devices is still relatively low, they indeed demonstrate substantially improved contact features.

Finally, we have studied both the structure and electrical properties of graphene films grown by chemical vapor deposition (CVD). Using dark field transmission electron microscopy (DFTEM), we found that such films are polycrystalline, consisting of many separate crystal grains stitched together by defect structures at the boundaries. Surprisingly, both the average grain size and grain boundary connectivity can be varied during synthesis. In fact, our samples with smaller grains actually exhibit the best stitching characteristics. Since defects are expected to hinder the flow of electric current, we then developed a novel experimental method combining DFTEM with transport measurements in order to

determine the electrical properties of individual grain boundaries in graphene. We discovered that the resistivity of grain boundaries is directly correlated with their structures, with those better connected physically exhibiting better electrical conductance overall. As a consequence of these findings, we were further able to demonstrate exceptional large-scale device performance using our best stitched samples rivaling that of exfoliated, single-crystal graphene, despite the marked polycrystallinity of these films.

8.2 Future Directions

In this final section, we shall discuss a few ideas for future studies on carbon nanotubes, pentacene thin films, and graphene beyond what was already mentioned in their respective chapters.

Carbon Nanotubes

In our photoelectrical studies of carbon nanotubes under zero bias conditions, we attributed the origin of the photo-induced current to the presence of local electric fields arising from electronic band bending. This is the same mechanism underlying current generation in photovoltaic devices. Similar studies have been conducted on graphene devices and qualitatively similar photocurrent features have been observed at the contacts (*1-3*). The origin of the photoresponse in graphene, however, is now believed to be a result of a unique photothermal effect, and not due to the photovoltaic mechanism (*4, 5*). As a result of these new findings, our studies on carbon nanotubes should be revisited. Ideally, the precise mechanism responsible for photocurrent

generation at the metal contacts and within the nanotube body ought to be clarified for both metallic and semiconducting nanotubes, as it could potentially depend on the electronic properties of the material.

Regardless of its precise nature, however, a different direction can be taken to supplement photocurrent studies of carbon nanotubes. While photocurrent microscopy has demonstrated great sensitivity to locate transport barriers caused by variations in the nanotube's band structure, it is not a direct probe for local resistance. Photothermal imaging also does not suffice in this regard, as it measures only the overall conductance of the device. In contrast, scanning probe techniques have clearly demonstrated this capability as we have already discussed in Section 1.5. It may be worthwhile to combine photocurrent microscopy with scanning probe measurements in the manner diagrammed in Figure 8.1. The two imaging modes will therefore provide complementary information on band structure and electrical resistance, allowing for a clear understanding of their relationship between the two.

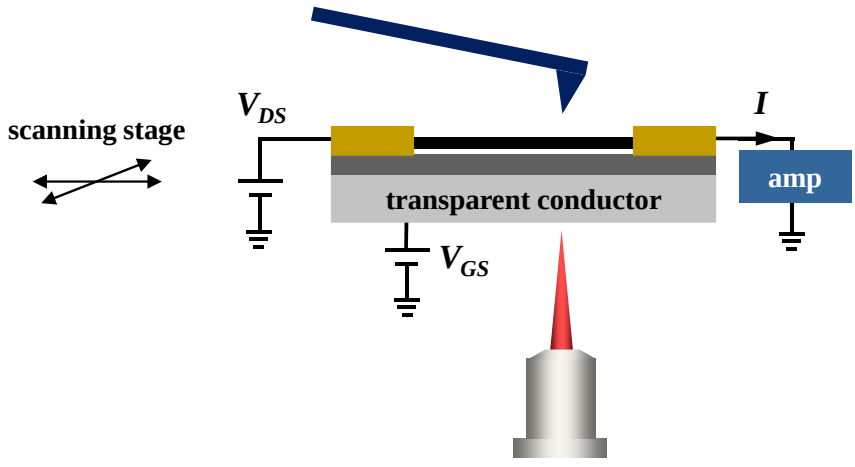

Figure 8.1 Schematic of experimental technique combining photocurrent microscopy with scanning probe microscopy.

Pentacene Thin Films

While pentacene islands tend to avoid nucleation in the vicinity of traditional metals like gold, we found that they readily grow across the graphene and silicon oxide interface. This finding points to an exciting advance in the development of nanoscale pentacene devices using graphene electrodes. When the dimensions of the pentacene channel can be made smaller than the average pentacene grain size, we expect such devices to consist largely of single grains. Previously, carbon nanotubes have been used to inject carriers into single pentacene islands (*6*). These devices showed much improved performance compared with those based on palladium contacts. We expect similar characteristics from the use of CVD graphene electrodes. However, in contrast to the former, such graphene-based devices should demonstrate greater scalability as well as uniformity, since nanotubes with different chiralities will themselves exhibit different transport behavior.

Finally, it is important to verify that individual pentacene islands indeed consist of single grains. As we learned from CVD graphene, this may not necessarily the case. Using our novel experimental scheme, we can study transport in pentacene devices fully characterized by DFTEM. The influence of individual grain boundaries may be investigated in this manner as well.

Graphene

Our discussion of graphene has been almost entirely limited to that of a single layer. However, CVD growth can often produce areas with multiple graphene layers (*7*). For bilayer graphene, there is rotational degree of freedom between the two

sheets. When both lattices are oriented in the same direction, the interaction energy is lowest in a configuration called *Bernal stacking*. In general, however, the two lattices can be rotationally offset with an angle between 0 and 30 degrees. It has been shown that for Bernal stacked bilayer graphene produced by mechanical exfoliation, there exists an electronic band gap that is tunable with the application of a vertical electric field (*8*), whereas rotated bilayer graphene is expected to show characteristics similar to that of isolated single sheets (*9*). It will be important to experimentally determine whether CVD grown bilayer graphene exhibits the same corresponding properties. Here, DFTEM can again be used to first explicitly determine the offset angle between the layers.

Finally, it is also known that Bernal stacking for bilayer graphene is not a unique configuration. Instead, there exist two mirrored stacking orders with degenerate energies that both are Bernal (*10*). Using DFTEM, Brown *et al.* found that in bilayer systems grown by CVD, both stacking configurations exist together, forming domains similar to grains in single-layer graphene (Figure 8.2) (*11*). However, the structure of the boundaries between these two stackings is not yet well understood. It is unclear whether they also consist of line defects, or if instead the two layers are physically translated with respect to one another there. In either case, we may use analogous experimental methods to understand the electrical properties of these domain boundaries.

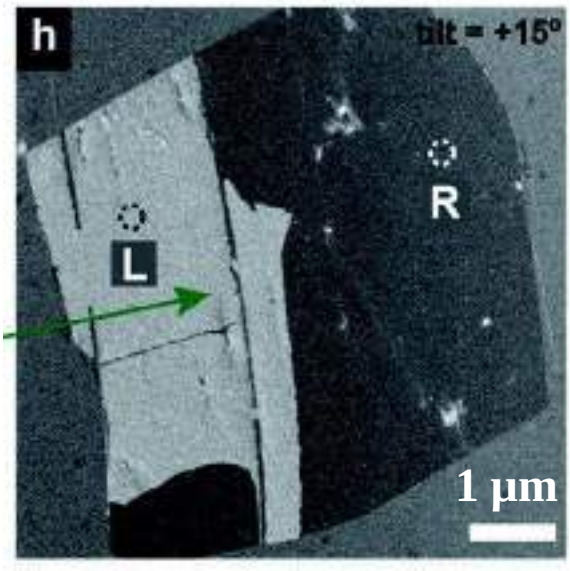

Figure 8.2 DFTEM image of Bernal stacked bilayer graphene grown by CVD. Bright and dark regions indicate domains with different stacking orders. Reproduced from (*11*).

8.3 Final Remarks

In this thesis, we focused on the study of three carbon-based nanomaterials that can potentially be used for electronic applications. In the past few decades, however, there has been an explosion in the development and exploration of a diverse array of nanomaterials, and we unfortunately cannot address all of them. While modern lithography technology can provide us with hands small enough to touch them, we also require the sight afforded by our various microscopes. Furthermore, we must be able to see and feel them simultaneously; otherwise we may never get to understand the elephant in its entirety.

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