Direct electron beam patterning of sub-5nm monolayer graphene interconnects

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ABSTRACT

The industry's march towards higher transistor density has called for an ever-increasing number of interconnect levels in logic devices. The historic transition from aluminum to copper was necessary in reducing timing delays while future technology nodes presents an opportunity for new materials and patterning techniques. One material for consideration is graphene, a single atomic layer of carbon atoms. Graphene is known to have excellent electrical properties [1], driving strong interest in its integration into the wafer fabrication processes for future electronics [2], and its ballistic transport properties give promise for use in on-chip interconnects [3]. This study demonstrates the feasibility of a direct electron beam lithography technique to pattern sub-5nm metallic graphene ribbons, without using a mask or photoresist, to act as next generation interconnects. Sub-5nm monolayer and multilayer graphene ribbons were patterned using a focused electron beam in a transmission electron microscope (TEM) through direct knock-on ejection of carbon atoms. These ribbons were measured during fabrication to quantify their electrical performance. Multilayered graphene nanoribbons were found to sustain current densities in excess of 10^9 A/cm^2, orders of magnitude higher than copper, while monolayer graphene provides comparable performance to copper but at the level of a single atomic layer. High volume manufacturing could utilize wafer-size chemical vapor deposition (CVD) graphene [4] transferred directly onto the substrate paired with a direct write multi-beam tool to knock off carbon atoms for patterning of nanometer sized interconnects. The patterning technique introduced here allows for the fabrication of small foot-print high performance next generation graphene interconnects that bypass the use of a mask and resist process.

1. INTRODUCTION

Industry's rapid approach towards single-digit nanometer nodes has generated an assortment of novel patterning techniques. Various next-generation technologies are under development, e.g. extreme ultraviolet lithography [5], block copolymers [6], direct ebeam writers [7] and nanoimprint lithography [8] to name a few. However, the march towards smaller devices requires not only lithography advances but also novel device designs and materials. The continued transistor scaling motivated the integration of SiGe strained silicon, high-κ/metal gate materials, and most recently the tri-gate transistor [9] that moves beyond planar technologies to allow increased switching performance and reduced leakage current. Likewise, the need for greater interconnect performance drove the use of copper for critical layers, replacing aluminum as the interconnect material. In this manuscript, we introduce a maskless resist-free patterning technique that was used to pattern a candidate material for post-copper interconnects: graphene nanoribbons.

Graphene, a single atomic sheet of sp^2 bonded carbon, has attracted an explosive growth of research ever since its isolation on SiO_2 in 2004 (Figure 1). Excellent electronic, mechanical and thermal properties make graphene a promising material for future electronics and applications in nanotechnology [10]. Specifically, the delocalized pi bonds of graphene allow its charge carriers to behave as two-dimensional massless Dirac fermions with mobilities $>10^4$ on SiO_2 at room temperature [11]. Graphene's unique transport properties have also attracted research for its use as a post-copper interconnect material [12].

Here, we present a proof of concept lithography technique similar to direct ebeam lithography [7], for fabricating sub-5nm graphene interconnects. Section 2 details how an aberration-corrected transmission electron microscope (AC-TEM) was used to achieve this patterning technique. Section 3 discusses the use of this technique to fabricate monolayer graphene interconnects, and section 4 presents the electrical measurements of sub-5nm interconnects fabricated from monolayer and

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multilayer graphene, revealing sustained current densities orders of magnitude greater than copper. These findings reinforce the value of R&D investment in graphene as a next generation interconnect material. Section 5 is a brief summary of the significant results in this manuscript.

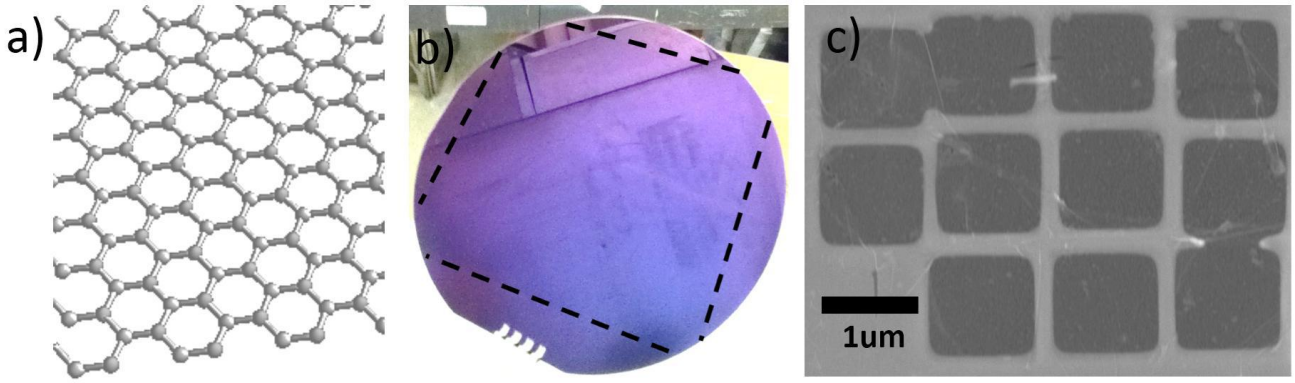

Figure 1: a) Ball-and-stick schematic of monolayer graphene. b) 4"x4" chemical vapor deposition (CVD) graphene sheet on Si wafer with 300nm SiO_2 capping layer. c) SEM micrograph of a sheet of CVD graphene suspended on top of an array of 1µm x 1µm square holes stamped into a 100nm thick free-standing Si_3N_4 membrane.

2. MASKLESS RESIST-FREE PATTERNING USING AN ELECTRON BEAM

Extending 193 nm immersion lithography to sub-20nm nodes has resulted in the need for multiple patterning techniques and a continued increase in required photomasks for critical layers [13-15]. Additionally, the need for aggressive optical proximity correction and inverse lithography technology exponentially adds to the mask complexity [16-18]. Similarly, photoresist development continually faces a resolution, line-edge roughness, and sensitivity (RLS) tradeoff that prevent significant improvements in all three areas simultaneously [19]. Here, we demonstrate the ability to pattern at nanometer-scale resolution while bypassing the necessity of a photomask and resist process.

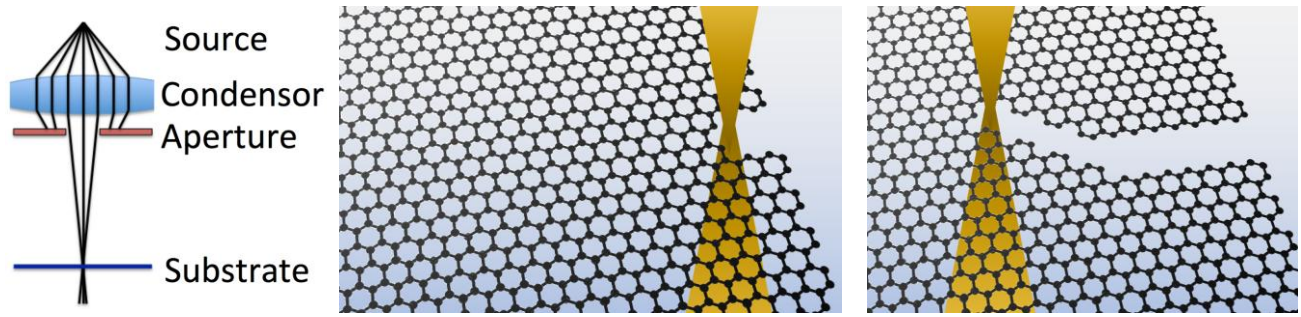

Figure 2: Schematic of the patterning technique using a focused electron beam within a TEM. The technique is applied to sculpt graphene interconnects by direct removal of carbon atoms from the graphene lattice.

A maskless resist-free electron beam patterning technique has been realized within a transmission electron microscope (TEM), where the focused electron beam was used to ablate and sculpt metals [20], and as well as suspended multi-layered graphene [21-22]. The focused beam (<5nm beam convergence) could be moved along a desired path, ablating the substrate, to form an arbitrary pattern (Figure 2). We extended this technique to an FEI Titan 80-300 field-emission aberration-corrected TEM (AC-TEM) that enabled nanometer-scale patterning paired with atomic-level imaging resolution. First, a suspended graphene sample was inserted into the AC-TEM (chip schematic in Figure 3a) and imaged at 300keV with atomic-level resolution (Figure 3b). The 2D FFT of the TEM micrograph (Figure 3c) revealed the structure of the monolayer graphene and its crystallographic orientation. It was also possible to distinguish between graphene islands on the surface and vacuum (holes), as seen from the varying edge contrast in Figure 3b.

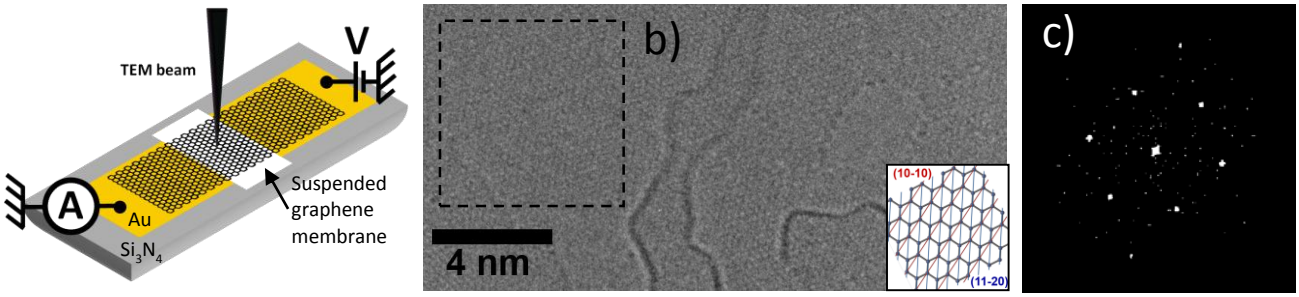

Figure 3: a) Schematic of device structure for nanosculpting of suspended monolayer graphene. b) High resolution image of device showing the lattice structure of a suspended graphene. Holes in the monolayer are observed and are distinguished from graphene islands on top of the sheet by the varying edge contrast. c) The 2D FFT of the square box in b) reveals crystallographic information from the 10-10 (2.13 Å) and 11-20 planes (1.23Å). Inset of b): schematic of the 10-10 and 11-20 planes of graphene.

Patterning was achieved using a 300keV electron beam, focused to its minimum diameter. The beam was shifted with magnetic lens deflectors to the area of interest, which could then be patterned into an arbitrary geometry by using the beam to knock carbon atoms from the graphene lattice. It has been reported that to structure graphene efficiciently, an acceleration energy >86keV is necessary to induce knock-on damage [23-24], however, sputtering of unsaturated carbon bonds is still possible at 50keV [25-27]. Figure 4a shows the creation of a sub-10nm nanopore within a multilayered graphene membrane, demonstrating the precision of this lithography technique. The series of TEM micrographs in figures 4b-4d demonstrates this sculpting process using a high resolution TEM (JEOL 2010F) at 200keV for patterning a narrow graphene constriction.

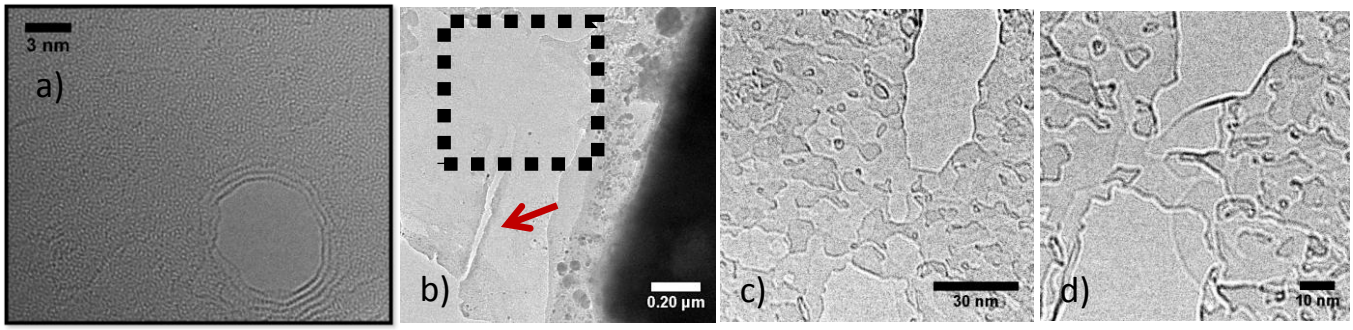

Figure 4: a) Nanopore created in suspended multilayer graphene using a focused electron beam within an AC-TEM. b) The result of sculpting a suspended graphene membrane (red arrow). c-d) Same device successively sculpted with an electron beam and then imaged, showing the control and resolution possible using this direct write technique.

3. PATTERNING OF SUB-5NM MONOLAYER GRAPHENE INTERCONNECTS

Samples were based on Si/SiN_x substrates obtained from WRS Materials. Self-standing SiN_x membranes of dimensions 50 µm x 50 µm were patterned using conventional techniques, and slits ~200nm wide were etched through the membrane using a focused ion beam. Large-area graphene grown by atmospheric pressure chemical vapor [28-29] was released from a copper growth substrate and transferred onto the Si/SiN_x wafer. The graphene layer was patterned into a free-standing ribbon geometry connected to large-area electrical contacts using standard electron-beam lithography. The sample was mounted on a TEM holder with electrical feed-throughs to allow simultaneous imaging and electrical transport measurements within the TEM (Figure 5). The focused electron beam was then used to progressively narrow the graphene ribbon from 500 nm to sub-10 nm, providing a platform to controllably sculpt and define the device geometry while measuring its electrical properties in-situ. Figure 5 shows the progressive reduction in width of a graphene ribbon from 500 nm to 45nm. During the sculpting, the ribbon is held at a bias voltage of 1V. Joule heating of the ribbon prevented the

adsorption of residual hydrocarbons onto the graphene surface. Nanoscale sculpting was achieved by manual control of the beam's location; it is also possible to implement a script to have the sculpting done under computer control.

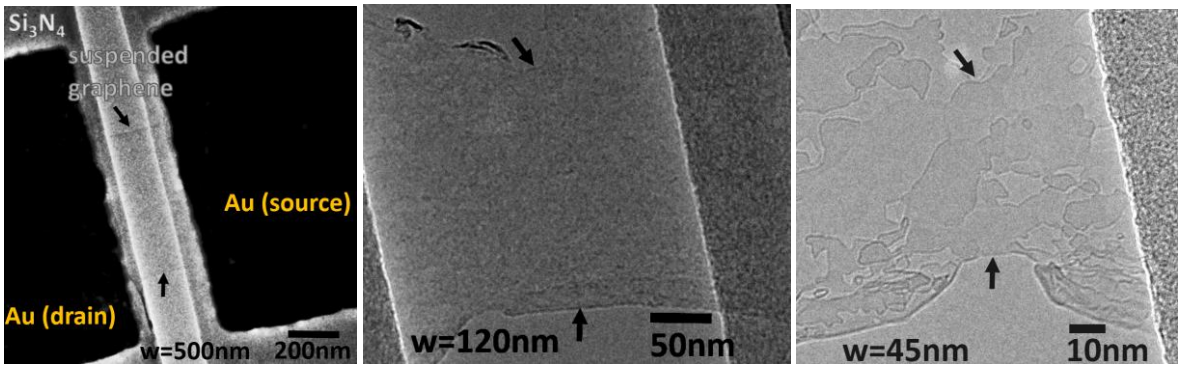

Figure 5: Successive narrowing of a suspended graphene ribbon from 500nm to 45nm using a focused electron beam withn an AC-TEM.

The sculpting procedure was used to produce graphene nanoribbons with widths less than 5 nm (Figure 6). For ribbons at this scale, imaging the graphene constriction induced heavy knock-on damage due to bombardment from the tightly focused, high current density 300keV ebeam. Thinning of the monolayer graphene ribbon via electromigration was possible through a careful control of the bias voltage. Figure 6 shows the progression of the ribbon narrowing to a width of ~1nm. To allow for greater control over the device geometry, an 80keV beam could be used to minimize structural damage during imaging.

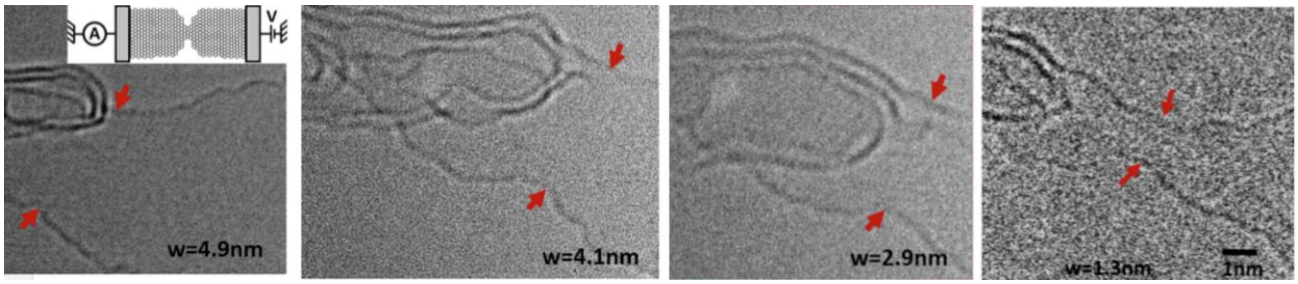

Figure 6: Narrowing of monolayer graphene nanoribbon from ~5nm to ~1nm. The ribbon is connected to source-drain electrical contacts to allow for simulatinous electrical biasing and transport characterization. Inset shows a schematic of the device layout. Arrows signify the minimum width of the nanoribbon.

4. RESULTS AND PROSPECTS OF GRAPHENE INTERCONNECTS

An important metric for interconnects is the maximum current density before device degradation or breakdown. The sample platform introduced here allows for in-situ electrical characterization of the imaged devices via electrical feedthroughs on the TEM holder. Figure 7a shows typical in-situ electrical measurements of a graphene ribbon until device breakdown. TEM micrographs of the devices were continuously captured until device breakdown, allowing for a quantitative correlation between the physical and electrical properties of graphene interconnects. Figure 7b shows a 5nm-wide multilayer graphene nanoribbon with its correlated electrical readout represented by the dotted line in Figure 7a. We observed current densities on the order of ~10^9 A/cm^2 for multilayer graphene <5nm in width, while for monolayer graphene, current densities of ~10^7 A/cm^2 were measured in the same width regime (Figure 7c).

To put things into perspective, the maximum current density for copper interconnects in advanced very large-scale integrated technology is on the order of 10^7-10^8 A/cm^2 [30]. In this regard, metallic multilayered graphene nanoribbons offer a factor of ~10-100 improvement in current density, while monolayer graphene provides comparable performance to copper but at the level of a single atomic layer.

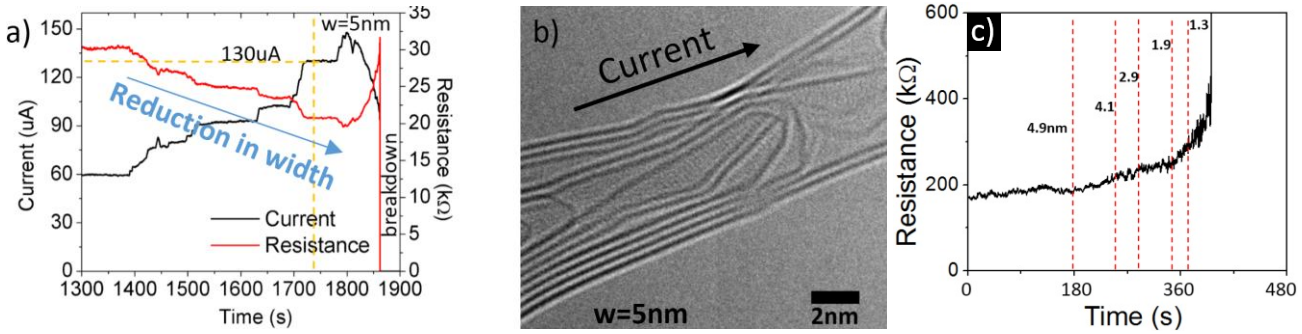

Figure 7: a) Electrical characterization of a multilayered graphene nanoribbon from a width of 8nm until breakdown. Dotted line represents the ribbon at width of 5nm sustaining a current of 130μA. b) Micrograph of the 5nm width graphene ribbon. c) Electrical characterization of a monolayer graphene nanoribbon from a width of 5nm until breakdown. Dotted lines and adjecent numbers represent the widths of the narrowing ribbon.

5. SUMMARY

High-resolution lithography using a focused electron beam within an AC-TEM was used to demonstrate the feasibility of patterning potential next-generation graphene interconnects down to single-digit nanometer widths without the use of a resist process or photomask. A 300keV electron beam was used to remove carbon atoms from the hexagonal lattice via direct knock-on damage, offering a path to sculpt and pattern graphene into arbitrary geometries. Sub-5nm monolayer and multilayered graphene ribbons were fabricated and electrically characterized within the AC-TEM to reveal a current density on the order of ~10^7 A/cm^2 and ~10^9 A/cm^2, respectively. The direct ebeam patterning technique and in-situ electrical transport measurements demonstrates both a novel nanometer-resolution patterning technique and graphene's potential as a post-copper interconnect material.

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