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Signal and Noise in FET-Nanopore Devices

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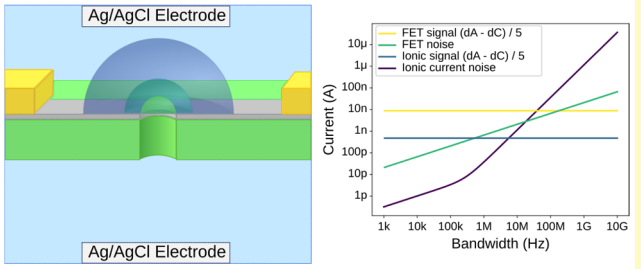
ABSTRACT: The combination of a nanopore with a local field-effect transistor (FET-nanopore), like a nanoribbon, nanotube, or nanowire, in order to sense single molecules translocating through the pore is promising for DNA sequencing at megahertz bandwidths. Previously, it was experimentally determined that the detection mechanism was due to local potential fluctuations that arise when an analyte enters a nanopore and constricts ion flow through it, rather than the theoretically proposed mechanism of direct charge coupling between the DNA and nanowire. However, there has been little discussion on the experimentally observed detection mechanism and its relation to the operation of real devices. We model the intrinsic signal and noise in such an FET-nanopore device and compare the results to the ionic current signal. The physical dimensions of DNA molecules limit the change in gate voltage on the FET to below 40 mV. We discuss the low-frequency flicker noise (<10 kHz), medium-frequency thermal noise (<100 kHz), and high-frequency capacitive noise (>100 kHz) in FET-nanopore devices. At bandwidths dominated by thermal noise, the signal-to-noise ratio in FET-nanopore devices is lower than in the ionic current signal. At high frequencies, where noise due to parasitic capacitances in the amplifier and chip is the dominant source of noise in ionic current measurements, high-transconductance FET-nanopore devices can outperform ionic current measurements.



KEYWORDS: *nanopore, nanoribbon, FET, DNA, sequencing*

A nanopore is a few-nanometer-diameter hole in a thin dielectric membrane. When immersed in an electrolyte solution, a voltage can be applied across the membrane to drive ions and charged molecules through the nanopore.[1−3] A molecule passing through the pore blocks part of the ion current, allowing the structure of the molecule to be read in a recording of the ion current. Solid-state nanopores have been used to study small molecules such as DNA, RNA, and proteins and have even shown promise for high-throughput, label-free DNA sequencing. However, the nanometer diameter of DNA molecules and the subnanometer separation between nucleotides constrain the magnitude of the blocked current signal that nanopores can produce. These constraints along with the fast translocation speeds (<1 μs dwell time of each nucleotide) and high-frequency amplifier noise[4,5] have thus far prevented solid-state nanopores from sequencing DNA.

In order to boost the signal and improve the high-frequency performance, an alternative detection scheme was proposed where a field-effect transistor would be placed near a nanopore (FET-nanopore).[6,7] These initial theoretical works modeled a graphene nanoribbon near a nanopore and calculated that DNA translocating through the nanopore would produce base-specific changes in the conductance of the nanoribbon. In these simulations, the nanopore only acted to localize the DNA molecule near the nanoribbon, and the conductance changes were solely due to charge coupling between the DNA and the nanoribbon.

The first experimental FET-nanopore devices that detected translocations of DNA through a nanopore used silicon nanowires.[8] However, the observed decreases in conductance due to DNA translocations did not match the expectation for a p-type semiconductor gated by negatively charged DNA. Due to small Debye lengths in physiological solutions, the FET response was not due to direct charge coupling to the DNA molecule. Instead, it was experimentally determined that the device amplifies local potential variations that arise when a DNA molecule constricts the ion current flow through the nanopore. Nanopores with graphene nanoribbon sensors have since been realized,[9−11] although crosstalk was attributed to the small signals seen in similar devices.[11] While theoretical modeling of the charge-detection mechanism has been performed, there has been little study of this local potential detection mechanism and its relation to the operation of real devices. Also, the signal and noise limitations in the ionic current have been studied,[4,12−15] yet the expected signals and noise in local FET devices have not been discussed. Here, we discuss the detection mechanism of the FET-nanopore device, its expected signals, and noise. We consider the dimensions of ssDNA to determine geometry of the ideal nanopore and the maximum resistive pulse signals it can produce. We calculate the change in voltage at the entrance of the nanopore and compare the result to the flicker, thermal, and capacitive noise in the device and amplifier.

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SIGNALS IN FET-NANOPORE DEVICES

First, we introduce nanopores and the signal associated with a molecule's translocation. In the simplest approximation, a nanopore is three resistors in series (Figure 1a). The interior of the nanopore is modeled as a cylindrical resistor, $R_p = {}^{4L}/_{\sigma\pi D^2}$, where σ is the conductivity of the electrolyte, L is the length of the nanopore, and D is its diameter. Additionally, there is an access resistance in series on each side where current paths converge from the bulk electrolyte into the pore,[16] $R_a = {}^{1}/_{2\sigma D}$. The total resistance of the nanopore is the sum of the tree resistances, the interior, and two access resistances

$$R_{tot} = R_p + 2R_a = \frac{1}{\sigma}\left(\frac{4L}{\pi D^2} + \frac{1}{D}\right) \quad (1)$$

When a molecule, like DNA, translocates through the nanopore, the molecule of diameter d blocks a cross-section of the nanopore, reducing the pore to an effective diameter

$$D_{eff} \approx \sqrt{D^2 - d^2} \quad (2)$$

and increasing the interior and access resistances. This resistance change is often detected by measuring the ion current through the nanopore, where dips in the ion current correspond to translocations:

$$\Delta I_{pore} = V_{ionic}\left(\frac{1}{R_{tot}(D)} - \frac{1}{R_{tot}(D_{eff})}\right) \quad (3)$$

where V_{ionic} is the transmembrane voltage. Alternatively, the resistance change can be detected by measuring a voltage difference in the three-resistor nanopore voltage divider.

A FET-nanopore device is a nanowire, nanotube, or nanoribbon that is placed near a nanopore, as illustrated in Figure 1c. The nanowire is the channel of the FET. A nanopore is drilled through the membrane, either next to the channel or through it. A bias is applied across the source-drain electrodes to drive a current through the channel. The channel is gated by the electrolyte, which is connected to the transmembrane Ag/AgCl electrodes. The nanopore provides a conductive path for the Ag/AgCl electrode on the opposite side of the membrane from the channel (bottom chamber in Figure 1c) to couple to the portion of the channel near the nanopore. In the simple circuit model, the FET gate is connected in between one of the access resistances and the internal pore resistance (Figure 1c inset). A translocating molecule that increases the pore and access resistances also reduces the coupling between the channel and the opposite side Ag/AgCl electrode. Thus, the translocation of molecules through the pore is measured as current changes in the channel. The change in voltage at the nanopore entrance (V_{en}) due to a molecule translocation can be modeled as

$$\Delta V_{en} = V_{ionic}\left(\frac{R_a(D)}{R_{tot}(D)} - \frac{R_a(D_{eff})}{R_{tot}(D_{eff})}\right) \quad (4)$$

The voltage falls as $1/r$ away from the pore entrance (Figure 2c), so the voltage sensed by the FET will be less than this.

The physical dimensions of the translocating molecule set the scale of the signals that can be produced by the nanopore. An ideal nanopore would be one that maximizes the signal, either by maximizing the change in ion current through the pore or by maximizing the change in voltage in the access region as a molecule translocates. The optimal geometry of the

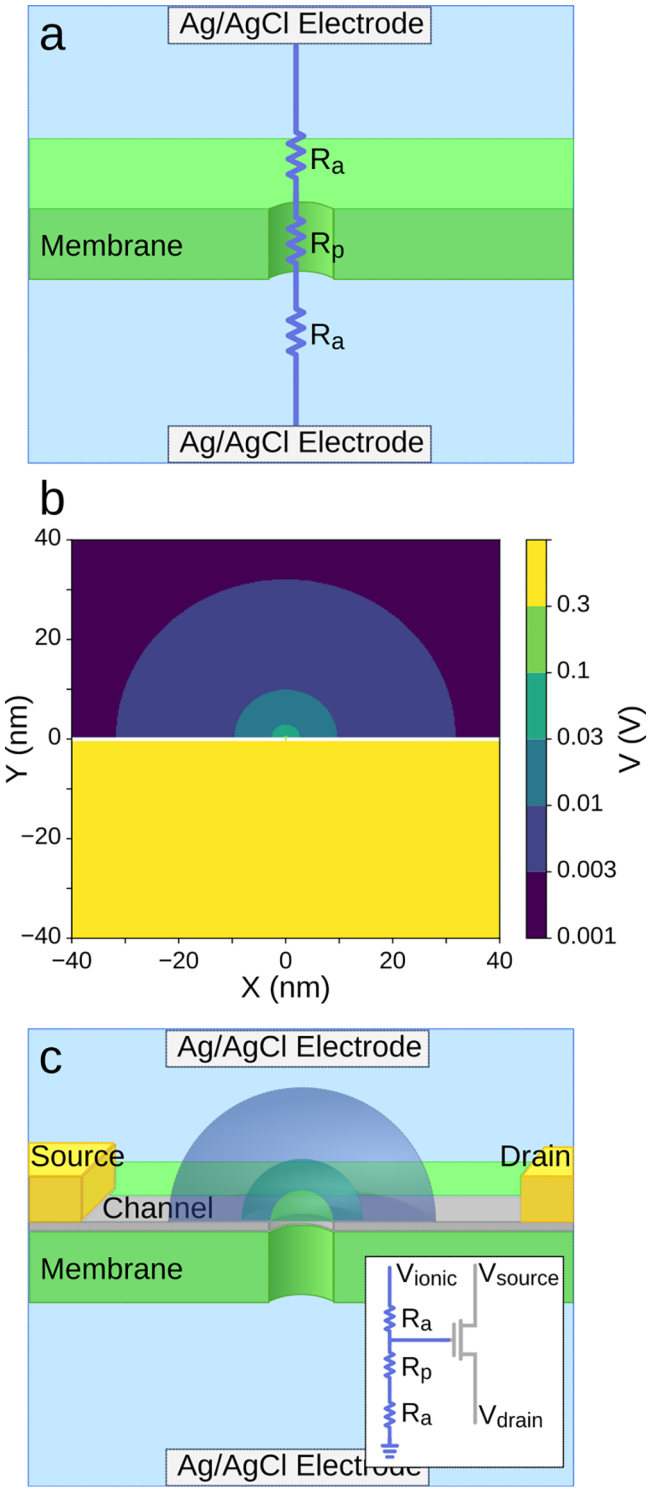

Figure 1. Schematic of a nanopore. (a) Drawing of a nanopore overlaid with a simple circuit schematic showing the access resistances and the interior resistance. (b) Plot of voltage profile, using a log scale, showing the voltage set by the electrode in the bottom chamber affecting the potential in the top chamber near the nanopore. Dimensions are D = 1.3 nm, L = 0.6 nm, and V_{ionic} = 500 mV. (c) Drawing of a nanopore with a local FET. The channel is in the access region of the nanopore such that it couples to the voltage set by the bottom Ag/AgCl electrode. Inset is the schematic of the FET-nanopore circuit.

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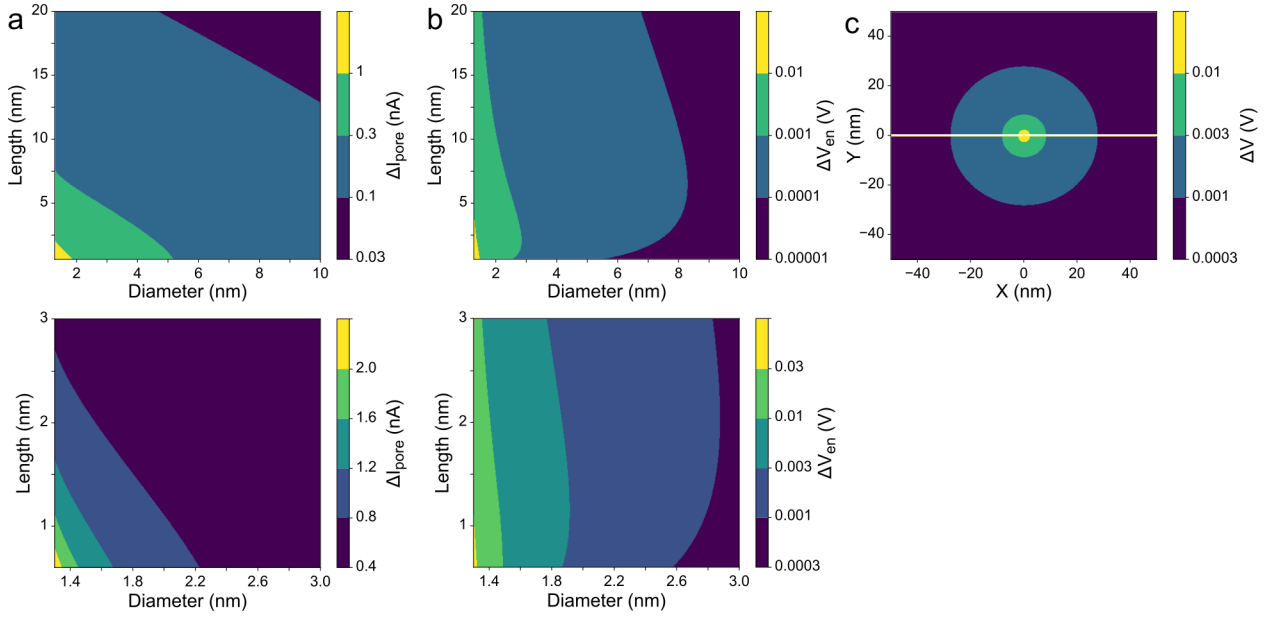

Figure 2. Nanopore signals due to ssDNA translocation versus pore geometry, assuming ionic voltage of 500 mV and an electrolyte conductivity of 30 S/m. (a) Difference in ionic current through the nanopore between $D_{eff}(dA)$ and $D_{eff}(dC)$. (Bottom) Same image over smaller length and diameter range. (b) Difference in voltage at the entrance of the nanopore between $D_{eff}(dA)$ and $D_{eff}(dC)$. (Bottom) Same image over smaller length and diameter range. (c) Profile of the change in voltage between $D_{eff}(dA)$ and $D_{eff}(dC)$ for a nanopore with dimensions D = 1.3 nm, L = 0.6 nm, V_{ionic} = 500 mV.

nanopore and the maximum signal achievable will depend on the experiment and the analyte. Because of the interest in nanopores for DNA sequencing, our discussion will focus on using a nanopore to distinguish adenine (dA) from cytosine (dC) in single-stranded DNA (ssDNA), but similar analysis could be performed for any analyte. The length of the nanopore is constrained by the separation between subunits in the analyte. Any portion of the molecule within the pore contributes to the signal, so the length of the nanopore must be reduced to or below the separation between subunits in the analyte. Atomically thin materials with thicknesses L < 1 nm can be used to get as close as possible to the separation between bases in DNA (≈ 0.34 nm). The transmembrane voltage is therefore limited by the separation between subunits. Too high a voltage will cause dielectric breakdown[17,18] or erosion of the nanopore wall. For atomically thin materials, the transmembrane voltage must be kept below 500 mV,[18−20] and often below 200 mV. The voltage change at the pore entrance due to a translocation, and similarly the change in ion current through the pore, is maximized when the diameter of the nanopore is as small as possible (Figure 2). The electrolyte must be compatible with the analyte. A high conductivity electrolyte is 3 M KCl, with a conductivity σ = 30 S/m.

To model the DNA molecule, we will compare the analyte diameters of adenine d(dA) ≈ 1.28 nm and cytosine $d(dC)$ ≈ 1.18 nm, where the sizes are estimated from current blockades of polyA and polyC homopolymers in thin SiNx nanopores.[21] The separation between bases in ssDNA is 0.34 nm, so we will use the effective length of a monolayer graphene nanopore L = 0.6 nm[19] as the physical limit of the thickness of a nanopore, regardless of the membrane material. Combining these constraints gives an ideal nanopore: V_{ionic} = 500 mV, σ = 30 S/m, D = 1.3 nm, and L = 0.6 nm. Using these values, the maximum blocked current and voltage signals due to a ssDNA translocation are ΔI_{pore} = 10 nA and ΔV_{en} = 100 mV, and the maximum signal differences between D_{eff}(dA) and D_{eff}(dC) (where D = 1.3 nm) are ΔI_{pore} = 3 nA and ΔV_{en} = 40 mV. Figure 2 shows the current change and voltage change at the pore entrance due to a ssDNA translocation for various sizes of nanopores. In protein nanopores as well as solid-state pores, the current blockades of each base do not always match this simple resistance model.[22] We will first use the simple resistor model to understand the signal and noise, then discuss deviations from this model.

The FET-nanopore device turns voltage changes in the access region of the nanopore into current changes in the channel. The transconductance of the FET, the channel current gained by changing the gate voltage, is therefore an important parameter. The potential in the access region falls as $1/r$ away from the entrance of the nanopore due to the geometry of the pore.[23] Therefore, most of the channel will not be gated by V_{en}, unless the channel is as small as the nanopore and right next to it. To express the transconductance in terms of the voltage at the entrance of the pore, we define an effective transconductance

$$g_{m,eff} = \frac{dI_{ch}}{dV_{en}} \tag{5}$$

Maximizing the $g_{m,eff}$ will maximize the DNA translocation signal in the FET.

In an experiment, the effective transconductance of the FET should be measured to ensure that an observed conductance change in the FET is due to coupling to the voltage in the access region of the nanopore and not crosstalk between the ionic and nanoribbon parts of the circuit.[11] The effective transconductance of the device can be measured by keeping the ionic voltage on the FET side of the membrane constant and sweeping the ionic voltage on the opposite side of the membrane while measuring the channel current. The applied transmembrane voltage can be scaled to the voltage at the entrance of the pore so that

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$$g_{m,eff} = \frac{R_{tot}}{R_a}\frac{dI_{ch}}{dV_{ionic}} \quad (6)$$

We recommend measuring the effective transconductance due to changes in voltage at the pore entrance as a control experiment. If an FET-nanopore device is gated by voltages in the access region, the channel current changes due to a DNA translocation should be

$$\Delta I_{ch} = g_{m,eff}\Delta V_{en} \quad (7)$$

As shown in Figure 2, ΔV_{en} can be estimated from the geometry of the pore and analyte, so channel current measurements can be estimated and compared to experimental data.

NOISE IN FET-NANOPORE DEVICES

Current noise in nanopores has been studied, especially low-frequency flicker noise.[12−15] Due to the high speed of ssDNA translocations (>10^6 bases per second), state-of-the-art nanopore amplifiers are still too noisy at the high bandwidth required to sequence DNA.[4] Since FET-nanopore devices are an alternative measurement of the changing nanopore resistance, we discuss here the low (<10 kHz), medium (<100 kHz), and high-frequency (>100 kHz) noise in FET-nanopore devices. We will distinguish between output noise of the nanopore (voltage fluctuations in the three-resistor nanopore circuit) and current noise in an FET-nanopore device. The signal-to-noise ratio (SNR) for a signal ΔI and a noise power spectral density of $S(f)$ is

$$\mathrm{SNR} = \frac{\Delta I}{\sqrt{\int_{f_{min}}^{f_{max}} S(f)\,df}} \quad (8)$$

where the measurement bandwidth is BW = $f_{max} - f_{min}$.

1/*f* Noise. Low-frequency flicker noise in an FET has a current power spectral density of

$$S_I(f) = \frac{AI_{ch}^2}{f} \quad (9)$$

where A is an empirical parameter that depends on the device, fabrication process, and operating conditions. The signal-to-noise ratio only considering this $1/f$ noise is

$$\mathrm{SNR} = \frac{g_{m,eff}\Delta V_{en}}{I_{ch}\sqrt{A\ln\frac{f_{max}}{f_{min}}}} \quad (10)$$

Rearranging, the FET-nanopore device must obey

$$\frac{g_{m,eff}}{I_{ch}} > \frac{\mathrm{SNR}\times\sqrt{A\ln\frac{f_{max}}{f_{min}}}}{\Delta V_{en}} \quad (11)$$

in order for the signal to be larger than the noise. To put this into perspective, the value of $\sqrt{A}$ in real devices ranges from 10^{-4} to 10^{-1},[24,25] $\sqrt{\ln\frac{f_{max}}{f_{min}}} < 10$ for any reasonable operating bandwidth, and the maximum ΔV_{en} < 40 mV discussed above, so for the signal of an FET-nanopore device to be larger than the flicker noise, we must have

$$g_{m,eff}\times 1\ \mathrm{V} > I_{ch} \quad (12)$$

Therefore, when operating an FET-nanopore device, the transmembrane voltage and source-drain voltage should be chosen to satisfy this relation. For example, if a current of I_{ch} = 1 μA is driven through the channel, the effective transconductance must exceed $g_{m,eff}$ > 1 μS by an amount that depends on the value of the flicker noise parameter A.

Thermal Noise. *Thermal Voltage Noise in the Nanopore.* The nanopore is a resistor and thus generates noise due to random thermal fluctuations, known as Johnson noise. The thermal voltage noise power spectral density is

$$S_V(f) = 4kTR \quad (13)$$

where k is Boltzmann's constant and T is the temperature of the resistor. If we consider only thermal noise, we can write the SNR at the input using the geometry of the nanopore and analyte, before we consider the noise any voltage detector will add. The thermal-noise limited bandwidth for a given SNR is then given by

$$\mathrm{BW} = \frac{(\Delta V_{en}/\mathrm{SNR})^2}{4kTR_{eq}(D_{eff})} \quad (14)$$

where, for the three-resistor nanopore model, the Thevenin equivalent resistance is

$$R_{eq} = \frac{R_a(R_a + R_p)}{R_{tot}} \quad (15)$$

Figure 3a plots the thermal-noise limited bandwidth for base differentiation with SNR = 5 for various pore geometries. This estimate predicts a maximum bandwidth of ≈100 MHz for SNR = 5, without considering noise added by an FET or any voltage measurement tool. Note that we ignore Joule heating that may occur at the high electric field and current density described by our ideal nanopore operated at a 0.5 V bias.[26,27] Joule heating may raise the thermal noise above what is estimated by using room temperature in eq 13 and reduce the estimate of the thermal noise limited bandwidth. We leave this for future study.

Thermal Current Noise in the FET-Nanopore Device. There will also be thermal current noise in the channel of an FET placed near a nanopore. When the FET is operated in the linear regime, the thermal current noise will be

$$S_I(f) = 4kTg_o \quad (16)$$

where g_o is the conductance of the channel. The translocation signal will be maximized when the transconductance is maximized. This can be achieved by operating the device in the saturation regime, at a high source-drain bias. In this regime, the current noise in the channel is

$$S_I(f) = 4kT\gamma g_m \quad (17)$$

where γ is a device-dependent parameter usually between 2/3 and 1. The voltage noise in the gate will also generate current noise in the channel, so the total thermal current noise in the channel in saturation is

$$S_I(f) = 4kTg_m^2R_{eq} + 4kT\gamma g_m \quad (18)$$

Thus, the thermal noise limited bandwidth of an FET-nanopore device is

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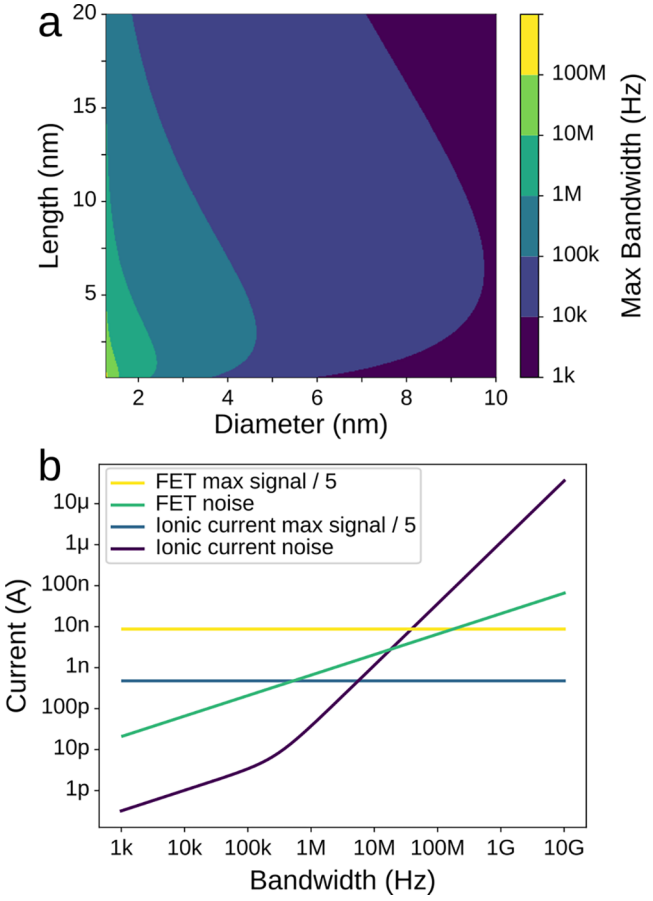

Figure 3. Bandwidth of FET-nanopore devices. (a) The thermal voltage noise bandwidth limit for detecting voltage differences between d(dA) and d(dC) with SNR = 5 for various pore geometries, using V_{ionic} = 500 mV. (b) Comparison of signal (difference between dA and dC, divided by 5) and integrated current noise between FET and ionic current measurements, using $g_{m,eff}$ = 1 μS and the ideal nanopore V_{ionic} = 500 mV, D = 1.3 nm, L = 0.6 nm, and σ = 30 S/m.

$$\mathrm{BW} = \frac{(g_{\mathrm{m,eff}}\Delta V_{\mathrm{en}}/\mathrm{SNR})^2}{4kTg_{\mathrm{m,eff}}^2 R_{\mathrm{eq}} + 4kT\gamma g_{\mathrm{m}}} \tag{19}$$

In the limit of infinite transconductance this equation becomes eq 14.

High Frequency Capacitive Noise. In state-of-the-art nanopore current amplifiers, capacitive noise dominates at frequencies above 100 kHz.[4] In these amplifiers, negative feedback opamp circuits are used in order to measure the current through the nanopore while keeping the voltage across the nanopore constant. This scheme leads to current noise with the spectral density of[13]

$$S_{\mathrm{I}}(f) = (2\pi C_{\mathrm{amp}}\nu_{\mathrm{n}})^2 f^2 \tag{20}$$

where C_{amp} is the total capacitance at the input of the amplifier (ignoring parasitic nanopore membrane[4,5] and source-drain capacitances) and ν_n is the input referred voltage noise. State of the art nanopore amplifiers have an amplifier noise constant of $C_{amp}\nu_n = 10^{-8}\ {}^{\mathrm{pA}}/_{\mathrm{Hz}^{3/2}}$.[4] This leads to a current noise of 1 nA at 10 MHz, surpassing the maximum SNR/5 in the ionic current signal below the average translocation speed of ssDNA.

The high-frequency response of an FET is limited by parasitic capacitances between the gate and source/drain electrodes, with a time constant on the order of

$$\tau_{\mathrm{parasitic}} \approx \frac{1}{g_{\mathrm{m}}} C_{\mathrm{gd}} \tag{21}$$

where C_{gd} is the parasitic gate-drain capacitance. Because the FET and the source and drain electrodes necessarily sit in the electrolyte solution, source and drain electrode passivation is extremely important for high-frequency performance. With a typical contact pad area of A > 100 μm^2 and g_m = 1 μS, the parasitic time constant is $\tau_{parasitic} = \epsilon_0 A/g_m t \approx 1000$ ns nm/t, where ϵ_0 is the vacuum permittivity and t is the thickness of the passivation between the electrolyte and the source/drain electrodes. The source and drain passivation needs to be at least 100 nm thick to reduce $\tau_{parasitic}$ below the average dwell time per base. However, if the contacts are well passivated, the intrinsic bandwidth of the FET can be increased so that the thermal noise still limits the bandwidth to 100 MHz.

DISCUSSION

This resistor model does not perfectly describe the working of a nanopore in all situations, for example when the nanopore membrane has a surface charge.[22,28] A surface charge on the nanopore membrane attracts mobile counterions to the edge of the nanopore, which can reduce the resistance of the nanopore and increase the ratio of the access resistance to the pore resistance, R_a/R_p. However, the voltage at the entrance of the nanopore is less sensitive to the changes in the ratio R_a/R_p as the ratio increases (eq 4), and the ratio is less sensitive to changes in the diameter of the analyte as the surface charge increases.[29] Therefore, we expect that increasing the surface charge on the nanopore will reduce the differentiation signal between dA and dC.

The salt concentration affects the conductivity of the electrolyte, the Debye screening length, and the capacitive coupling between the FET and the electrolyte. When using the same salt concentration on each side of the nanopore membrane (symmetric salt), reducing the salt concentration amounts to scaling the pore interior and access resistance terms equally. In the voltage divider, eq 4, equal increases in pore and access resistances cancel, so the voltage change signal at the nanopore entrance is not affected by the salt concentration. Reducing the salt concentration increases the resistance of the nanopore and therefore increases the thermal noise. Also, reducing the salt concentration will increase the Debye length and double layer capacitance and therefore reduce the effective transconductance of the FET. Therefore, the best SNR in the FET signal should be obtained at high salt concentrations.

The salt concentration can be lowered on just one side of the membrane (asymmetric salt) in order to increase only one resistance in the three resistor voltage divider. We can modify eq 4 by increasing the resistance of one of the access resistances by a factor α and increasing the pore resistance by a factor β to get

$$V_{\mathrm{en}} = V_{\mathrm{ionic}} \frac{\alpha R_{\mathrm{a}}}{\beta R_{\mathrm{p}} + (1+\alpha)R_{\mathrm{a}}} \tag{22}$$

with the conditions $\alpha > \beta > 1$. To first order, the voltage change signal at the entrance of the pore due to a small change in the diameter of the analyte (Δd) is given by

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$$\Delta V_{en} = \frac{\partial V_{en}}{\partial d}\Delta d \quad (23)$$

Decreasing the salt concentration on only one side of the membrane can boost this signal by increasing one access resistance relative to the other and to the pore interior resistance. Dividing the signal by the thermal noise gives the SNR for small changes in the diameter of the analyte. To compare this signal using asymmetric salt to the signal using symmetric salt, we calculate the ratio

$$\frac{SNR_{asymmetric}}{SNR_{symmetric}} = \frac{\beta}{\sqrt{\alpha}}\left(\frac{R_p + 2R_a}{\beta R_p + (1+\alpha)R_a}\right)^{3/2} \times \left(\frac{R_p + R_a}{\beta R_p + R_a}\right)^{1/2} \quad (24)$$

This ratio is less than 1 for all α and β. Although the voltage change signal can be boosted by using an asymmetric salt concentration, the thermal noise also increases due to increasing pore and access resistances. The signal-to-noise ratio is maximized in the symmetric salt case. The reduced salt concentration on the FET side of the membrane would also reduce the capacitive coupling of the FET to the voltage change signal, so the SNR in the FET would be further reduced.

The changing pore and access resistances due to a translocating analyte can be measured either by measuring the ion current, ΔI_{pore}, through the nanopore or by measuring the voltage in the access region, ΔV_{en}, with a local FET. These are complementary measurement schemes, so it is useful to compare the signal-to-noise performance and bandwidth limitations of each. Figure 3b shows a plot of the signal and noise as a function of measurement bandwidth, for $g_{m,eff} = 1\ \mu S$. In the thermal noise dominated regime (<1 MHz), the SNR in the ionic current is higher than the SNR in the FET current signals. For differentiating dA and dC, the SNR = 5 thermal voltage noise limited bandwidth for detecting changes in voltage in the access region (eq 14) is ~100 MHz, while the thermal current noise limited bandwidth for detecting changes in the ionic current is ~2 GHz. It is in the high-frequency, capacitive noise limited regime (>100 kHz), where amplifier current noise dominates the ionic signal, that the SNR in the FET-nanopore can be higher than in the ionic signal.

CONCLUSION

We have studied signal and noise in FET-nanopore devices and determined signatures of the voltage divider detection mechanism that are expected using realistic experimental parameters. FET current signals should scale linearly with transmembrane voltage, and they should also scale linearly with the effective device transconductance. Modeling an ideal nanopore for distinguishing bases in a ssDNA strand, the maximum voltage change signal at the nanopore entrance is on the order of 40 mV. At low frequencies, the SNR in ionic current measurements will always be greater than the SNR for voltage measurements. However, at high frequencies where capacitive noise currents dominate the ionic signal, large transconductance FETs can improve the maximum bandwidth over the ionic current signal, up to 100 MHz.

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Notes

The authors declare no competing financial interest.

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