CdSe nanocrystal quantum-dot memory

M. D. Fischbein and M. Drndic[a)]
Department of Physics and Astronomy, University of Pennsylvania, Philadelphia, Pennsylvania 19104

(Received 4 January 2005; accepted 4 April 2005; published online 3 May 2005)

Memory effects in the electronic transport in CdSe nanocrystal (NC) quantum-dot arrays have been observed and characterized. Conduction through a NC array can be reduced with a negative voltage and then restored with a positive voltage. Light can also be used to restore or even increase the NC array conduction. We have studied the switching of the conduction in CdSe NC arrays and found the behavior to be highly sensitive to the value and duration of the laser and voltage pulses. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1923189]

Undoped semiconductor CdSe nanocrystal (NC) arrays have been found to be highly insulating.[1,2] Due to the nanometer-size scale of the NCs, quantum confinement effects play a dominant role in their electronic properties. Individual CdSe NCs have discrete energy levels separated by ~100 meV and charging energies ~150 meV.[2] CdSe quantum dots are capped with ~1 nm thick organic ligands which act as tunnel barriers for charge transport between adjacent dots. Time-dependent transport phenomena, history effects and persistent photoconductivity in CdSe NC arrays have been observed.[1–4] Proposed models to explain these effects include charge traps,[1] the Coulomb glass,[2,4] and Lévy statistics.[5]

In this letter, we study memory effects in the electronic transport in colloidal undoped CdSe NC quantum dot arrays. Conduction through a NC array can be reduced by applying a negative voltage and then reset with a positive voltage. Light can be used to reset or even to increase conduction in the NC array. The switching of the conduction in CdSe NC arrays is highly sensitive to the value and duration of the laser and voltage pulses. The ability to controllably switch NC array conduction can be exploited to fabricate memory devices composed of CdSe NCs. Such devices may be advantageous for several reasons. (i) Production of large quantities of CdSe NCs is easy and inexpensive. (ii) CdSe NC spectra are dependent on the NC size, which may allow selective memory resetting with visible light in devices composed of different size NCs. For instance, in a device composed of red and blue NCs, green light will reset the red NCs but not the blue NCs. (iii) As described in this letter, NC memory is robust, rewritable, and persists for long times.

To study the memory effects, field-effect transistors (FETs) composed of organically capped CdSe and CdSe/ZnS NCs were fabricated. Devices consisted of monodisperse TOPO-capped NCs, 3 to 6 nm in diameter, with a root-mean-square (rms) size dispersion <5%. NCs are either drop casted or spin coated onto the device from a highly concentrated hexane-octane solution and dried in a vacuum. The NCs self-assemble between 1 mm long Au electrodes, separated by ~2 μm on top of a 300 nm thick silicon oxide and a conductive gate below the oxide (Fig. 1).[2] The NC film thickness was varied from a few to hundreds of NC layers.

The measurement setup consisted of a cryostat operated from 1.5 K to 800 K. Silver-soldered teflon-coated wires were used as electrical leads to the device and the sample stage was made from Cu and Macor. NCs were annealed in a vacuum at ~600 K to 650 K for 1 h *in situ* and measured at 300 K and 77 K. Annealing *in situ* decreases the separation between the NCs and increases the conductivity[4] to a magnitude comparable with that of *n*-doped CdSe NCs.[6] NCs were photoexcited with a 532 nm wavelength (green) diode laser operating at ~1 mW/cm^2. Figure 1 shows the current-voltage curves of a device with 5 nm CdSe NCs at 300 K and 77 K in the dark and during photoexcitation. Voltage was applied to the source electrode and current was measured at the drain electrode with a current amplifier; the gate was grounded. For this FET geometry, the photocurrent curve is nearly symmetric while the dark-current curve is highly asymmetric. Hysteresis is seen in both cases and is inversely proportional to the voltage sweep rate. The dark current is ~0 for $V>0$, while for $V<0$ electrons contribute to transport.[2] A constant negative voltage generates a current transient in the NC array which decays as a power law in time; specifically, $I(t)=I_o t^a$, where $-1<a<0$.[2,4]

NC memory was probed with the four-step voltage sequence shown in Fig. 2. We label the four steps as; (1) Write, (2) wait, (3) read, and (4) erase to illustrate the potential for NC-based memory technology. The step durations are t_{write},

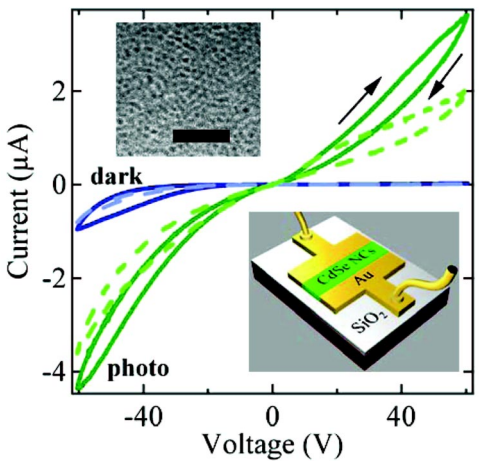

FIG. 1. Current-voltage curves at 300 K (dashed lines) and at 77 K (solid lines) for an array of 5 nm TOPO-capped CdSe NCs in the dark and during excitation with green laser. The voltage sweep rate is 1 V/s. Upper inset: Transmission electron micrograph of the NC film. The scale bar is 50 nm. Lower inset: Device schematic; 1 mm long electrodes are separated by 2 μm. The back gate is grounded.

[a)]Electronic mail: drndic@physics.upenn.edu

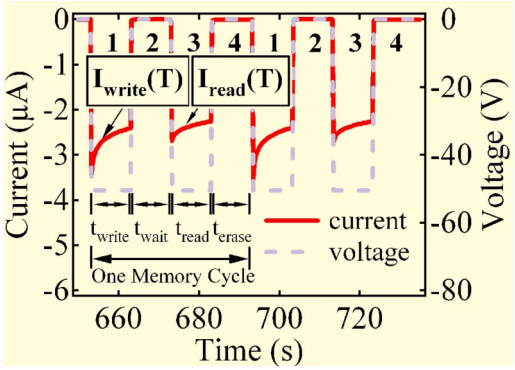

FIG. 2. Voltage (dashed line) and current (solid line) vs time for two consecutive memory cycles for the device in Fig. 1. The numbered steps are: (1) write ($V<0$, dark), (2) wait ($V=0$, dark), (3) read ($V<0$, dark), and (4) erase ($V=0$, photoexcitation) or ($V>0$, dark). In this example, $t_{write}=t_{wait}=t_{read}=t_{erase}=10$ s and $V=-50$ V during t_{write} and t_{read}. In Step 4, NCs were photoexcited. $I_{write}(T)$ and $I_{read}(T)$ are currents at time T after the start of the write and read steps, respectively.

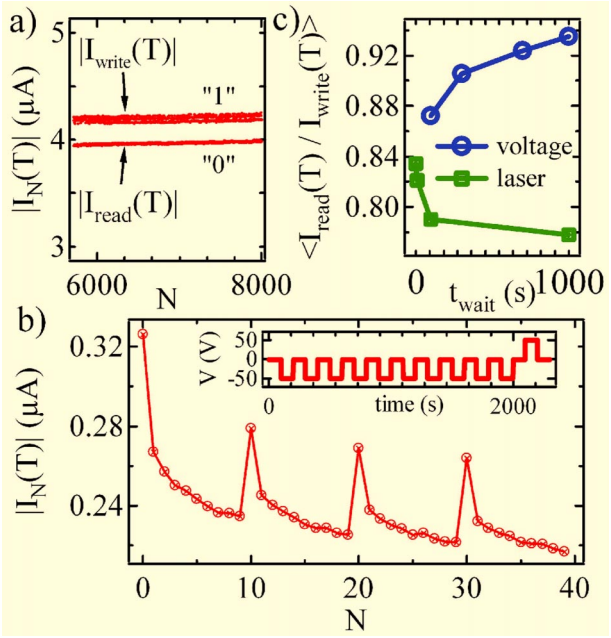

FIG. 3. (a) $|I_N(T)|$ vs the transient number, i.e., the number of the negative voltage steps, N, for 1000 consecutive memory cycles. $I_N(T)$ is the current at time T after the application of the Nth negative voltage step. $I_{write}(T)$ and $I_{read}(T)$ correspond to even and odd values of N, respectively (see Fig. 2); $t_{write}=t_{read}=t_{erase}=1$ s, $t_{wait}=3.5$ s, $T=500$ ms, $V=-50$ V, and photoexcitation was used to erase. (b) $|I_N(T)|$ vs the transient number, N, for consecutive memory cycles modified to have nine read steps per cycle; $t_{write}=t_{wait}=t_{read}=t_{erase}=100$ s, $T=500$ ms, $V=-50$ V, and positive voltage was used to erase. Inset: Voltage vs time for one modified memory cycle ($N=0$ to 9). (c) The average value $\langle I_{read}(T)/I_{write}(T)\rangle$, calculated over consecutive iterations, vs t_{wait} for positive voltage erasing (circles) and photoexcitation erasing (squares).

t_{wait}, t_{read}, and t_{erase}, respectively, and the current transients during the write and read steps are $I_{write}(t)$ and $I_{read}(t)$, respectively; $I_{write}(T)$ and $I_{read}(T)$ are the currents at time T after the start of their corresponding voltage steps. This four-step cycle will be referred to as the *memory cycle*. The first three steps are the voltage pulses $-|V|$, 0, and $-|V|$. As shown in Fig. 2, this generates the current transient sequence, $I_{write}(t)$, 0, and $I_{read}(t)$, respectively, where $|I_{read}(t)|<|I_{write}(t)|$. In the fourth step, either a positive voltage is applied *or* photoexcitation is induced with visible light at $V=0$. This fourth step is used to *reset* or *erase* the memory so that a subsequent application of $-|V|$ will generate $I_{write}(t)$ again. We measured memory cycles for electric fields from 0 to 30 V/μm; t_{write}, t_{wait}, t_{read}, and t_{erase}, were each varied from 1 s to 1000 s. Measurements were performed for both positive voltage and visible light resetting. In all cases, $|I_{read}(T)|<|I_{write}(T)|$. Memory was exhibited at both 300 K and 77 K for all voltages. The results shown are for 77 K and $E=-2.7\times10^5$ V/cm across the device.

Figure 3(a) shows $|I_{write}(T)|$ and $|I_{read}(T)|$ for 1000 consecutive memory cycles from the device in Fig. 2. Here, $T=500$ ms, $t_{write}=1$ s, $t_{wait}=3.5$ s, $t_{read}=t_{erase}=1$ s and photoexcitation was used in the erase step. As shown, $|I_{read}(T)|<|I_{write}(T)|$ and both are nearly constant over thousands of iterations ($\sim$2 h). To illustrate the potential of CdSe NCs for memory applications, $I_{write}(T)$ and $I_{read}(T)$ can be defined as two states, "1" and "0," respectively. The difference $\Delta I(T)=|I_{write}(T)-I_{read}(T)|\sim0.2$ μA is sufficiently large to avoid overlap of "1"s and "0"s due to current fluctuations ($\sim$10 nA). $\Delta I(T)>0.1$ μA for all t_{write}, t_{wait}, t_{read}, and t_{erase}. The memory properties are robust. The device in Fig. 1 was probed with thousands of voltage pulses over 3 months and no measurable degradation was observed.

Reversible switching of the current between 1 and 0 states in Fig. 3(a) can be explained by charge trapping in the NC array. During negative voltage pulses, electrons are injected into the array and some get trapped. Coulomb interactions between charges in CdSe NC arrays are unscreened and allow the trapped electrons to repel new electrons from entering the array, which reduces conduction. A positive voltage pulse removes trapped charges and therefore enhances conduction. This interpretation is supported by Fig. 3(b) which shows memory cycles modified such that $I_{read}(T)$ is measured nine times before the NCs are reset (by positive voltage). The number of trapped charges increases with each additional negative voltage pulse and each set of nine $I_{read}(T)$ values show monotonic decrease. In each cycle, the positive voltage used in the erase step removes most but not all of the trapped charges that accumulate during the single write step and the nine read steps. The currents in the subsequent cycles are therefore lower [Fig. 3(b)]. Even without the positive voltage step, trapped charges are able to diffuse out of the NC array during the wait step, when $V=0$ across the array. As t_{wait} increases, the number of charges which escape during this step increases. This is reflected in the upper curve (circles) in Fig. 3(c) showing the average ratio $\langle I_{read}(T)/I_{write}(T)\rangle$ plotted against t_{wait}. As expected, $\langle I_{read}(T)/I_{write}(T)\rangle$ increases as t_{wait} increases. As t_{wait} approaches infinity, all of the trapped charges diffuse out of the array and $\langle I_{read}(T)/I_{write}(T)\rangle$ approaches unity.

The lower curve in Fig. 3(c) shows $\langle I_{read}(T)/I_{write}(T)\rangle$ versus t_{wait} when photoexcitation at $V=0$ is used as the erase step. As shown, $\langle I_{read}(T)/I_{write}(T)\rangle$ decreases as a function of t_{wait}, which is the opposite of the behavior for positive voltage erasing. It was shown in Fig. 1 that the photocurrent is significantly larger than the dark current. Photoconductivity has previously been shown to persist in thin films of CdSe NCs for up to 10^4 s after exposure to light.[1] This mechanism of persistent photoconductivity explains the lower curve in Fig. 3(c). Persistent photoconductivity is at its maximum immediately after the photoexcitation erase step ends, and then

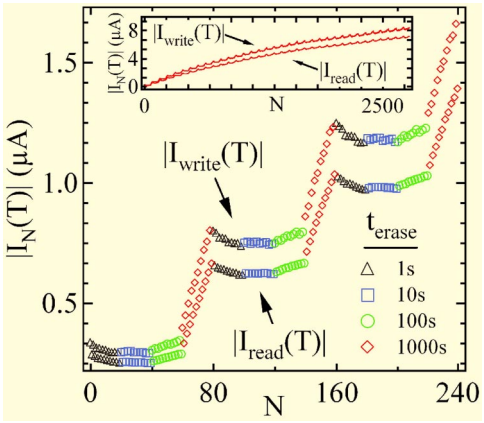

FIG. 4. $|I_N(T)|$, the current at time T after the application of the Nth negative voltage step vs the transient number, N, for consecutive memory cycles with laser resetting (Fig. 2); t_{erase} changes every ten cycles from $t_{erase}=1$ s (triangles), to 10 s (squares), 100 s (circles), and 1000 s (diamonds). After ten $t_{erase}=1000$ s memory cycles, t_{erase} is set back to 1 s and the entire 40-step sequence is repeated; $t_{write}=t_{wait}=10$ s, $T=500$ ms, and $V=-50$ V. The first three repetitions of these 40-step sequences are shown. $I_{write}(T)$ and $I_{read}(T)$ correspond to even and odd values of N, respectively (see Fig. 2). In one 40-step sequence N increases by 80. Inset: $|I_N(T)|$ vs the transient number, N, for ~35 repetitions of 40-step sequences (~120 h).

decays. $I_{read}(T)$ is measured at a time $\tau=t_{write}+t_{wait}+T$ after the erase step ends. As τ increases, the persistent photoconductivity decreases and $|I_{read}(T)|$ decreases. The lower curve in Fig. 3(c) can therefore be interpreted as a measurement of the decay of persistent photoconductivity.

When photoexcitation is used to erase NC memory, the effect of persistent photoconductivity can be used to "tune" the NC array's response to the write and read steps. If many memory cycles are measured consecutively, increasing (decreasing) t_{erase}, i.e., the duration of photoexcitation at $V=0$, will increase (decrease) $|I_{write}(T)|$ and $|I_{read}(T)|$ with each iteration of the memory cycle. To demonstrate this effect, t_{write} and t_{wait} were held constant while t_{erase} (by photoexcitation) was varied. First, t_{erase} was set to 1 s and then increased by one order of magnitude after every ten memory cycles, up to $t_{erase}=1000$ s. After ten $t_{erase}=1000$ s cycles, t_{erase} was set back to 1 s and the entire 40-step sequence was repeated. Three consecutive 40-step sequences are shown in Fig. 4 for $t_{write}=t_{read}=t_{wait}=10$ s. As shown, the slopes of the two lines, $|I_{write}(T)|$ and $|I_{read}(T)|$, change periodically with each repetition of the 40-step sequence. The slopes are negative for $t_{erase}=1$ s (i.e., $t_{erase}/t_{write}<1$), nearly zero for $t_{erase}=10$ s ($t_{erase}/t_{write}=1$) and positive for both $t_{erase}=100$ s and $t_{erase}=1000$ s ($t_{erase}/t_{write}>1$). The increase (decrease) of the slopes as t_{erase}/t_{write} increases (decreases) was observed for all parameters. The slopes and the ratio t_{erase}/t_{write} for which the slopes change sign, depend on t_{wait} and the laser power. As shown in Fig. 4, the current increase for $t_{erase}=1000$ s is greater than the current decrease for $t_{erase}=1$ s and there is, therefore, a net increase of the current. After ~120 h of repeating these 40-step cycles, the current was increased by nearly an order of magnitude.

In conclusion, colloidal CdSe NCs show robust memory effects that can be exploited for memory applications. NC memory can be erased electrically or optically and is rewritable. CdSe NC memory devices can be scaled down. For example, for a 100 nm gap, the voltage required to obtain similar currents is ~3 V.

The authors thank D. Novikov for useful discussions. This work was supported by the ONR Young Investigator Award No. N000140410489 and the ACS PRF award. One of the authors (M.F.) acknowledges funding from the NSF IGERT Program.

[1]D. S. Ginger and N. C. Greenham, J. Appl. Phys. **87**, 1361 (2000).
[2]N. Y. Morgan, C. A. Leatherdale, M. Drndic *et al.*, Phys. Rev. B **66**, 075339 (2002).
[3]W. Woo, K. Shimizu, M. V. Jarosz *et al.*, Adv. Mater. (Weinheim, Ger.) **15**, 1068 (2002).
[4]M. Drndic, N. Y. Morgan, M. V. Jarosz, M. A. Kastner, and M. Bawendi, J. Appl. Phys. **92**, 7498 (2002).
[5]D. S. Novikov, M. Drndic, L. S. Levitov *et al.*, cond-mat/0307031.
[6]D. Yu, C. J. Wang, B. L. Wehrenberg *et al.*, Phys. Rev. Lett. **92**, 216801 (2004).