Supporting Information

Improving signal-to-noise performance for DNA translocation in solid-state nanopores at MHz bandwidths

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1. Estimating the chip capacitance from geometrical considerations

To calculate C_{chip}, we split the chip capacitance in a set of capacitors of equal thickness, each one containing several dielectric layers, which are added to form the total capacitance. The capacitance of each of these regions is formed as the series of the capacitances associated with each layer.

We consider a 5-mm-by-5-mm chip with a 5-μm SiO_2 layer and a 100-nm SiN membrane. The SiN window size is 25 μm by 25 μm, the thinned area is 100 nm by 100 nm and 10-nm thick, and the glass slide is 200-μm thick and has a 100-μm- diameter hole. The silicone (average thickness of 0.5mm) is painted over all chip surfaces, except a 1 mm^2 large area around the nanopore.

The relative permittivities ε_r for the SiO_2, SiN, glass, and silicone are 4, 7, 4.7 and 2.5. The resulting capacitance for each region,as they are referred to in Fig. 2a, are C_1 = 0.85pF, C_2 = 0.13 pF, C_3 = 0.050pF, C_4 = 0.37 pF, and C_5 = 0.0013 pF , yielding a total chip capacitance C_{chip} = 1.42 pF, which compares favourably with the measured values for this chip.

2. Measuring chip capacitance

To compare the calculated capacitance in Fig. 2 to measured values, chip capacitance was measured in a fluidic cell with the VC100 low-noise patch-clamp amplifier (Chimera Instruments, New York, NY). Fig. S1 shows the ion current as a function of time measured while applying a triangle wave voltage bias at a frequency of 30 Hz with a slope α = 16 V/s across the nanopore (dashed black line in Fig. S1).

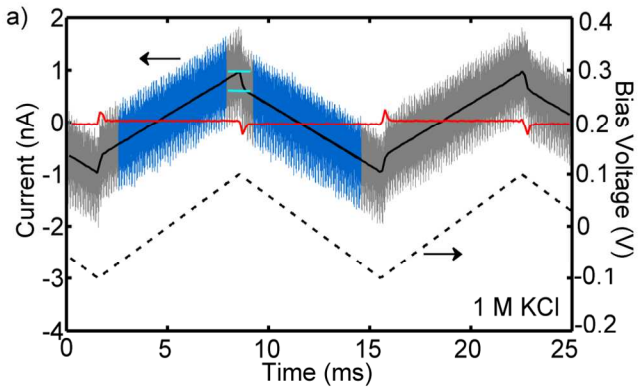

Figure S1. Measured ion current as a function of time in response to a 30 Hz triangle voltage wave (dashed line) across a nanopore chip in 1M KCl solution (blue at a bandwidth of 1 MHz, black at a bandwidth of 10 kHz, derivative indicated in red). The capacitance is calculated from the current step (ΔI, indicated in light blue) when the slope of the applied voltage changes from positive to negative (or negative to positive).

To calculate the chip capacitance, we model the nanopore chip by a resistor R_{pore} in parallel with a capacitance C_{chip}. The ion current response can then be expressed as $I = \frac{V(t)}{R_{pore}} + C_{chip}\frac{dV(t)}{dt}$. For a triangular wave voltage, the current is then the sum of a triangular wave from the resistive component (first term) and a square wave from the capacitive component (second term).

Figure S1 shows the ion current *vs.* time. By fitting the positive and negative slopes of the current traces one obtains ΔI at the point at which the derivative of the applied bias changes sign. The capacitance is then determined by $C_{chip} = \Delta I/2\alpha$, where α is the magnitude of the slope of the applied bias (16 V/s). The values for C_{chip} measured in this way are in excellent agreement with those calculated from geometrical considerations.

3. Estimating chip capacitance from the current power spectral density

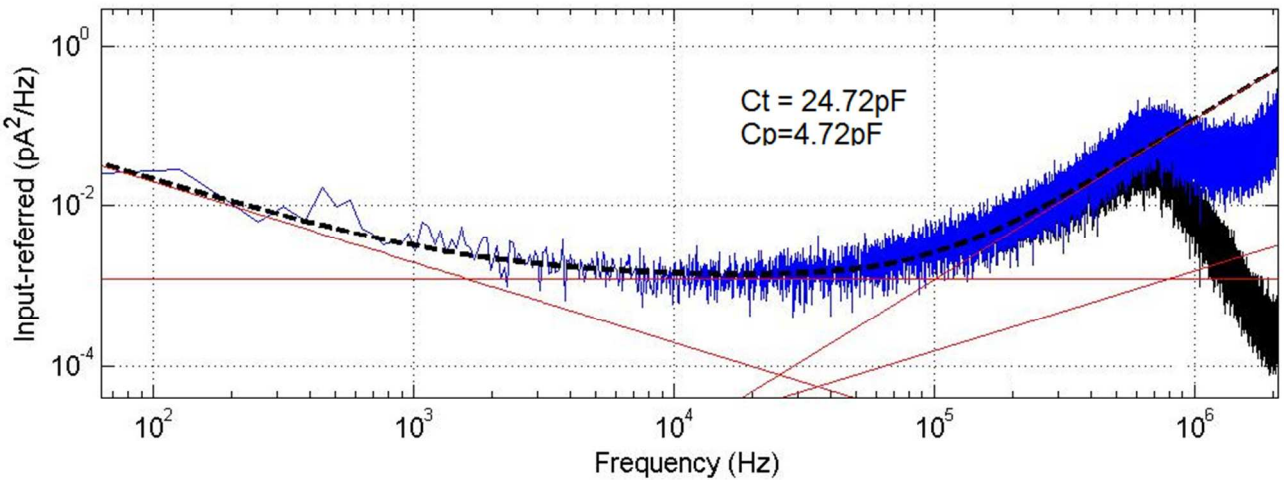

Figure S2. Input-referred power spectral density (PSD) of the ion current noise as a function of bandwidth for a chip with C_{chip} = 4.7 pF.

Fig. S2 shows the input-referred power spectral density (PSD) of the ion current noise as a function of bandwidth for a chip with C_{chip} = 4.7 pF. From fitting of the noise power spectral density (PSD) in Fig. S2 with the equation in the main text we can extract C_T = 24.7 pF and extract a capacitance of 4.7 pF for the chip, in good agreement with the values measured from the triangle-wave method.

4. Glass slide micro-positioning

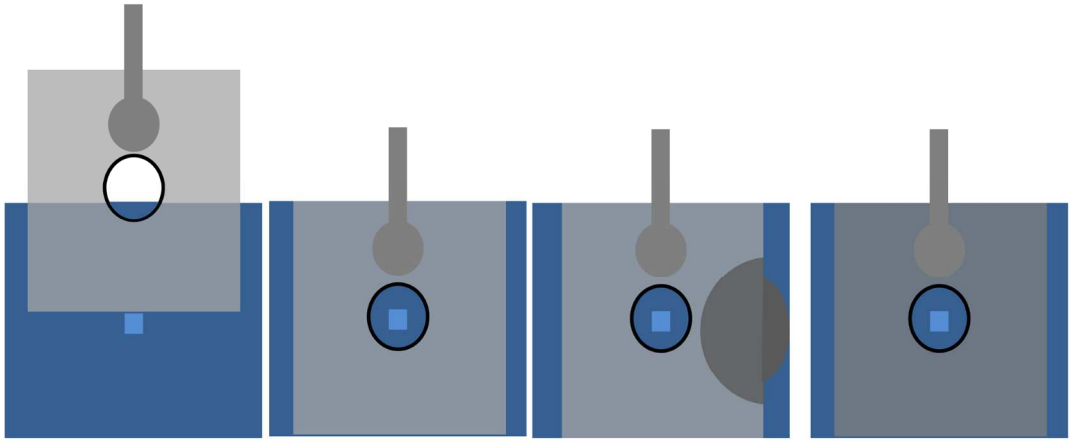

Figure S3. Glass slide positioning with a micromanipulator and bonding polymer expansion under the glass slide.

Fig. S3 schematically illustrates the process of glass bonding on silicon nitride nanopore chips. The glass is attached to the micromanipulator tip using a vacuum and then, underneath a microscope, aligned with the membrane. A small amount (less than one microliter) of adhesive is then dripped onto the surface of the chip using a wire brush. When it expands across the hydrophilic surface of the chip, it eventually reaches the edge of the glass and is pulled underneath it by capillary forces. If the correct volume of adhesive is used, it remains entirely underneath the glass, leaving the pore in the glass unobstructed.