In Situ Transmission Electron Microscopy Modulation of Transport in Graphene Nanoribbons

Supporting Information

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SI-1: TEM graphene characterization.

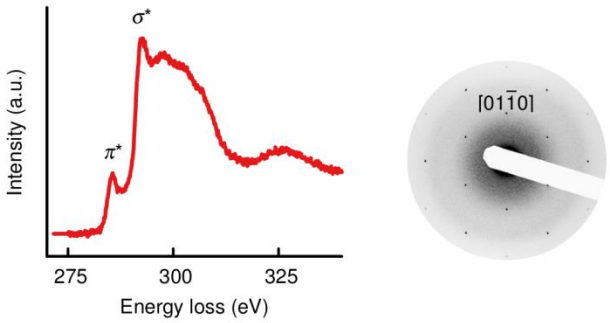

Figure SI-1: Energy electron-loss spectrum showing the carbon *K*-shell ionization edge (left) and electron diffraction pattern from a freestanding graphene strip fabricated in a TEM-compatible chip (right). Both signals were taken from an area ~ 0.5 μm^2.

SI-2: Graphene annealing *via* Joule heating.

Graphene was annealed within the TEM column *via* Joule heating by applying a voltage V_b between source and drain electrodes. The voltage was cycled in small increments up to 3 V to obtain current densities of the order of 10^{12} A m^{-2}. Above these values the devices failed. Annealing caused a drop in GNR resistance and morphology changes in the GNRs associated with contamination removal and crystallization of amorphous carbon.

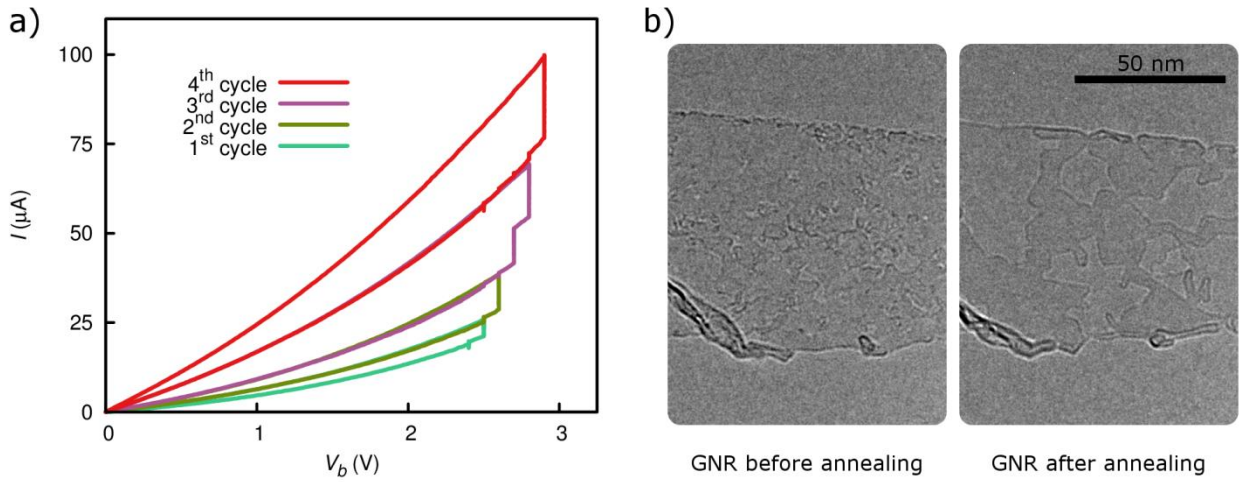

Figure SI-2: GNR annealing via Joule heating. a) Four annealing cycles in a 113-nm-wide GNR showing a decrease in GNR resistance as the V_b is increased. b) TEM images of a GNR before and after annealing showing morphology changes.

SI-3: Calculation details of the electrostatic potential and electric field.

The electrostatic potential V and electric field $\boldsymbol{E} = -\nabla V$ were numerically solved for vacuum ($\nabla^2 V = 0$) between the three electrodes (source, drain and gate) considering the electrodes' surfaces as boundary conditions with equipotential values. The gate potential was set to V_g while source and drain electrodes where grounded ($V = 0$). In the geometric model the electrodes' thickness is 50 nm except for the side-gate extension, carved from graphene in the experiment, whose thickness was set to 1 nm. The SiN_x film was omitted from this analysis. Numerical solutions of the electrostatic equations were obtained with a physics modeling software (COMSOL Inc.).

SI-4: Transport measurements details and leakage current analysis.

Graphene nanoribbons were connected to a voltage source (DAQ card National Instruments 6221) and a preamplifier to measure the current. A separate voltage source (multimeter Keithley 5417A) was used to supply the side-gate voltage. A custom LabVIEW program was used to set/sweep the voltages in addition to recording the electrical measurements. The leakage current $I_{leakage}$ of each device was established by measuring the current between gate and drain electrodes as a function of gate voltage V_g. In our measurements we capped $I_{leakage}$ to approximately ± 30 nA by limiting the V_g to a ± 10 V range, outside of which the low-stress 100-nm-thick SiN_x film becomes more permissible to current. All quoted currents I and, consequently, conductances G in the main text were obtained after $I_{leakage}$ subtraction.

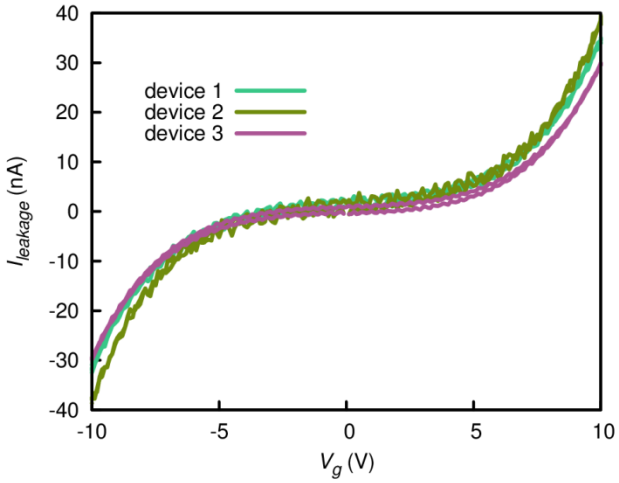

Figure SI-3: Leakage current between gate and drain electrodes as a function of gate voltage Vg from three independent devices.