Electronic Transport in Heterostructures of Chemical Vapor Deposited Graphene and Hexagonal Boron Nitride

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Graphene is a candidate material for an array of nanoelectronic applications, due to its favorable physical properties, including superior carrier mobility[1,2] and thermal conductivity,[3,4] high current breakdown density,[5,6] and compatibility with integrated circuit (IC) fabrication.[7,8] Progress in wafer-scale growth of highly crystalline graphene films provides a potential route towards commercialization of high-quality graphene-based electronics.[9,10] However, carrier transport in graphene is often significantly degraded by surface charge traps and impurities,[11–13] roughness due to the substrate[14] or intrinsic graphene rippling,[15] and charged vibrational modes[16] associated with commonly used SiO_2 substrates. Extrinsic carrier scattering by substrate phonons limits graphene's room temperature mobility to ca. 40,000 $cm^2\ V^{-1}\ s^{-1}$, significantly reduced compared to the intrinsic mobility in excess of 200,000 $cm^2\ V^{-1}\ s^{-1}$ that is expected due to acoustic phonon scattering alone.[17] The constraining effects of SiO_2 drive interest in substrate engineering, specifically the introduction of hexagonal boron nitride (hBN) dielectrics to improve graphene performance. Due to its robust, planar, and predominantly covalent bonding, hBN is expected to be atomically smooth, free of dangling bonds and charge traps, and chemically inert, with a bandgap of 5.97 eV and a slight ~1.7% lattice mismatch to graphene.[18] Dean et al. used exfoliated films for the first demonstration of significant enhancement of graphene-hBN heterostructures, reporting carrier mobilities of 60,000 $cm^2\ V^{-1}\ s^{-1}$ – three times larger than similar devices on SiO_2.[19] Chemical vapor deposited (CVD) graphene has also been characterized on exfoliated hBN layers, with room temperature mobilities in excess of 14,000 $cm^2\ V^{-1}\ s^{-1}$.[20,21] However, exfoliation is not a scalable process, so there remains a need to introduce a platform that allows for substrate engineering at the wafer-scale.

Recently, CVD growth of hBN has been demonstrated,[22–25] providing a route towards scalable, large-area fabrication of graphene-hBN heterostructure devices. In this work, we provide a systematic study to inform practical design considerations for hBN integration and report record low- and high-field transport in CVD-grown graphene-hBN heterostructure devices. A novel methodology was used to minimize the presence of contaminants in between layers of the graphene-hBN stack, allowing for continuous sheets of CVD-grown monolayer hBN to be consecutively stacked beneath CVD-grown monolayer graphene in intimate contact. The crystallographic orientation between the 2D materials is also controllable, allowing for well-defined stacking orientation and material thickness, advancing beyond previous methods.[23,24] High-vacuum current-annealing was utilized to lower the contact resistivity and vaporize surface contaminants from the fabrication process of CVD graphene-hBN heterostructures, resulting in hole and electron mobility values in excess of 8,000 $cm^2\ V^{-1}\ s^{-1}$, more than twice that of previous reports.[23,24] Finally, improved high-temperature (power dissipation) and high-bias (breakdown current density) performance were observed in graphene-hBN heterostructures and attributed to the effect of the 200 times greater thermal conductivity of five-layer hBN as compared to a SiO_2 substrate[26] and the higher energy optical phonon modes.[19]

Figure 1 is a schematic of the fabrication process, which is based on transferring and stacking of monolayer materials using a single PMMA resist scaffold to minimize contamination, similar to a recent report.[27] Device fabrication began with separating monolayer graphene from its copper growth substrate using a PMMA layer for mechanical support.[28–30] Metal nanoparticle contamination introduced during etching of the growth substrate was avoided by utilizing the bubbling transfer method.[28,31] The PMMA-graphene stack was subsequently cleaned in multiple deionized water baths and transferred directly onto a sample of monolayer hBN grown by CVD on a catalytic copper substrate, with the goal of preventing the introduction of unwanted contaminants (e.g., resist residue) between the graphene and hBN. This process was repeated until the graphene was supported by five hBN layers. We note that this transfer process allows for layer-by-layer control of the heterostructure thickness and could be utilized to define twist angles between crystalline 2D materials by orienting known edge structures (crystallographic orientation)

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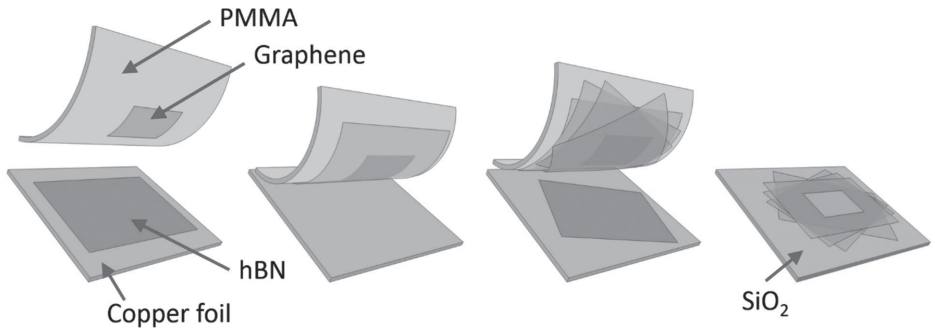

Figure 1. Schematic of the low-contamination process for graphene-hBN stacking and transfer.

of single flakes with micromanipulators under an optical microscope[19,32] (i.e. zig-zag edged hexagonal graphene,[30] Sulfur-terminated MoS_2,[33] triangular WS_2,[34] and others), advancing beyond previous methods.[27] A final transfer to a SiO_2/Si substrate and removal of the PMMA scaffold using acetone left the desired graphene-hBN heterostructure for patterning into device structures. Electron beam lithography (EBL) was used to pattern 1-μm wide electrodes in the transfer length method (TLM) configuration,[35] with channel separations ranging from 500 nm to 6 μm. A 3 μm-wide graphene ribbon was defined via a second round of EBL followed by oxygen plasma etching (see Figure S1 in the Supplementary Information). Fabrication of graphene devices on SiO_2 for TLM measurements followed the same lithographic process flow.

Microscopic characterization of finished devices is presented in **Figure 2**. Figure 2a is an optical micrograph of a 3-μm wide graphene ribbon on an oxidized silicon substrate, contacted in the TLM configuration. SEM micrographs indicated that the dimensions of the TLM channels were consistent with the design pattern (Figure 2c). Raman maps of device

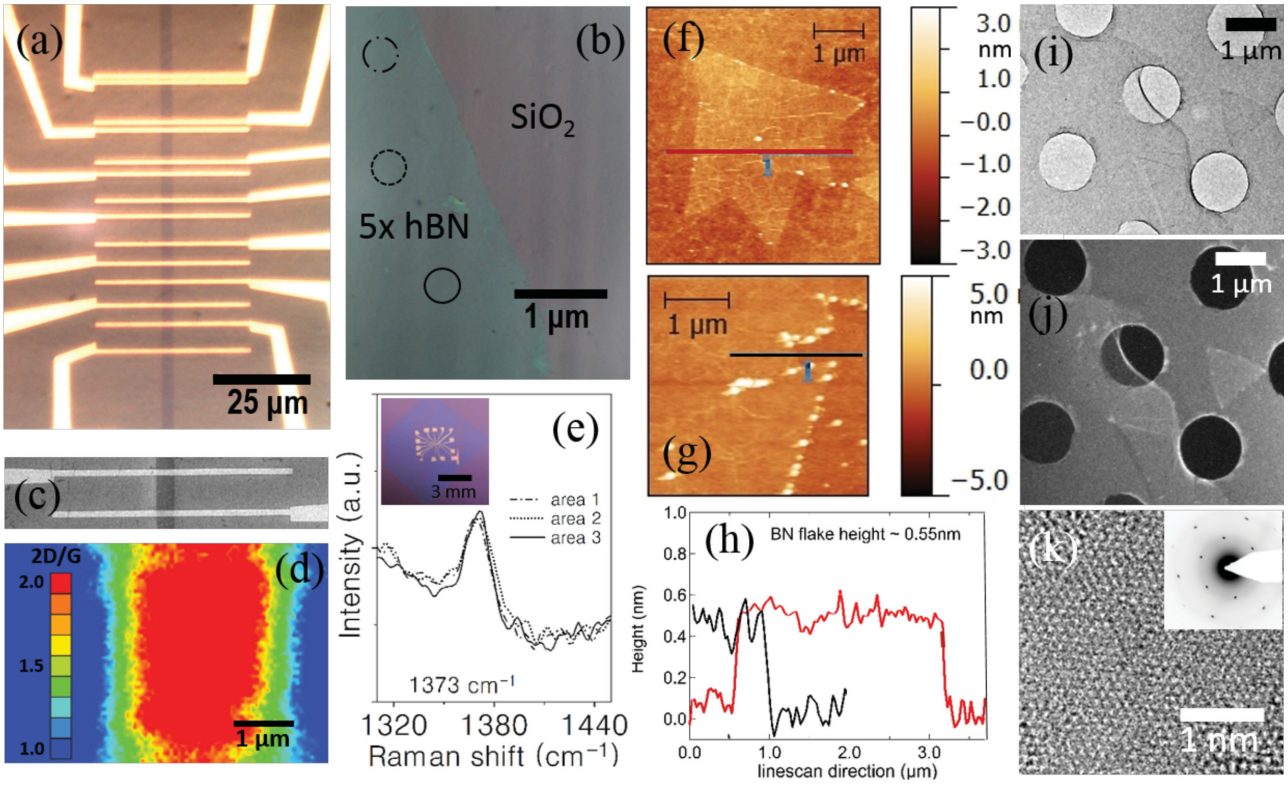

Figure 2. Characterization of CVD graphene/hBN and fabricated devices. (a) Optical micrograph of a 3-μm wide graphene ribbon contacted in the TLM configuration. (b) Optical micrograph of five-layer CVD hBN on SiO_2, with no graphene layer. Raman spectra from the three circled regions are presented in panel (e). (c) SEM image of a 3-μm graphene ribbon contacted by source and drain electrodes. (d) Raman map (2D/G ratio) of the channel region of a graphene ribbon. (e) Three Raman spectra of five-layer CVD hBN taken from the three areas circled in panel (b). All spectra show the peak centered near 1373 cm^{-1}, which is characteristic of monolayer hBN. Inset: Optical micrograph of patterned CVD graphene devices supported by a five-layer CVD hBN stack (appears darker as compared to SiO_2). (f) AFM image of a CVD hBN flake on SiO_2. (g) AFM edge morphology of a CVD hBN large-are sheet on SiO_2. (h) Corresponding height profile as extracted from line scans in (f) and (g). The observed step height of approximately 0.5 nm confirms that the sample is a monolayer. (i) Bright-field TEM image of CVD hBN showing a very clean surface. (j) Dark-field TEM image of (i) shows single crystal domains with size ca. 1 μm. (k) High resolution TEM image showing atomically pristine monolayer hBN. Inset: Electron diffraction showing six-fold intensity peaks in monolayer hBN.

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channels on SiO_2 were consistent with expectations for high-quality monolayer graphene, with 2D/G ratios consistently ~2 (Figure 2d).[36–38] An optical micrograph of a five-layer hBN stack (without graphene) on a 300 nm SiO_2 substrate is shown in Figure 2b. A design based on five layers of hBN was specifically chosen to effectively screen graphene carriers from dangling bonds associated with the oxide and to provide an atomically smooth surface (roughness <100pm).[19] Furthermore, a stack of five layers of BN has been shown to provide sufficient insulation from oxide charge traps (>1 GΩ).[39] Figure 2e shows corresponding Raman spectra from three distinct regions highlighted by circles in Figure 2b. The peak at 1373 cm^{-1} is representative of hBN and demonstrates uniform coverage of the hBN across the transferred area, consistent with our past report.[22] Atomic force microscopy (AFM) analysis of CVD-grown hBN flakes (Figure 2f) and sheets (Figure 2g) transferred on SiO_2 shows clean, monolayer hBN with triangular domains ~1 μm in size, low surface roughness, and a layer thickness of ~0.5 nm (Figure 2h). Interestingly, Figure 2g provides evidence that contaminant material is attracted to the edge of hBN monolayer sheets. We further characterized the hBN with aberration-corrected transmission electron microscopy (AC-TEM). For TEM analysis, hBN samples were transferred onto an amorphous carbon grid with 1-μm holes (Figure 2i). Consistent crystal orientation was observed across the suspended regions. Figure 2j shows the dark-field (DF) TEM image of Figure 2i, taken with one diffraction beam fixed at an atomic plane spacing of 0.12 nm. Crystallographic continuity is observed for domains ~1 μm, consistent with AFM findings. A high resolution TEM image of the hBN surface (Figure 2j) shows a pristine surface morphology, as expected from the a low-contamination (bubble) transfer process. A single six-fold diffraction pattern is observed (inset Figure 2k), consistent with AFM height measurements showing that the samples are monolayers (Figure 2h). All the data are consistent with a very clean transfer process of high quality monolayer hBN with crystal domains ~1 μm in size. We therefore expect intimate contact between stacked 2D materials attracted by Van der Waals forces.[40] An optical image of the final graphene-hBN device stack contacted in the TLM configuration is presented in the inset of Figure 2e.

Current-annealing was performed on a set of devices under high vacuum (10^{-6} Torr) with a slow voltage ramp (~5 mV/s) to 3 – 4 V in order to use Joule heating to vaporize contaminants from the lithography process and to improve the contact resistance.[41] **Figure 3**a shows typical I-V characteristics for the current-annealing process where the device was held at

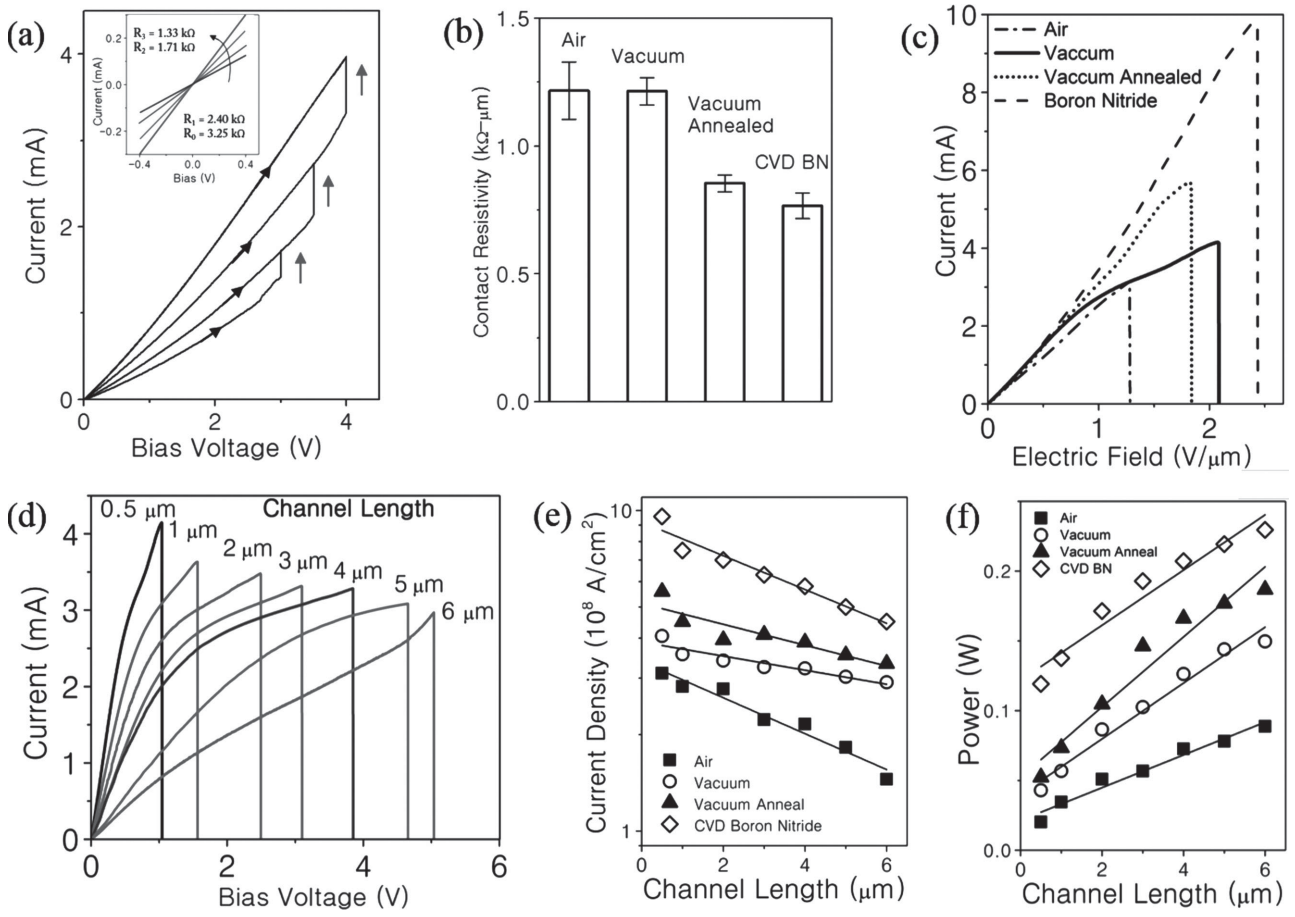

Figure 3. Current-annealing and breakdown characteristics of devices in the TLM configuration. (a) Current-voltage traces of consecutive high vacuum current-annealing runs on the same graphene device. Bias is held at 3.0 V, 3.5 V, and 4.0 V for 30 min. (b) Contact resistivity extracted from TLM measurements showing a ~30% decrease after current annealing. (c) Comparison of device breakdown at high-fields for devices with a channel length of 500 nm. (d) Typical breakdown characteristics of graphene ribbons of varying channel length. (e) Maximum current density of devices before breakdown. (f) Sustained power before device breakdown.

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3, 3.5, and 4 V to anneal the graphene at progressively higher temperatures. From the TLM measurements, it was found that this current annealing process caused the device resistance to decrease from ~3.3 kΩ to ~1.3 kΩ (inset Figure 3a) while the contact resistivity decreased from ~1.2 kΩ-μm to ~0.8 kΩ-μm (Figure 3b; see Figure S2 in Supplementary Information). The measured contact resistivity of ~0.75 kΩ-μm for annealed devices on hBN was approximately the same as that found for annealed devices on SiO_2 (Figure 3b), suggesting that the use of hBN as a substrate does not strongly affect the quality of the graphene-Cr/Au contact.

To inform development of future design rules for graphene-hBN device integration for both low- and high- field applications, we provide comparisons between various device configurations. A systematic study of high-field transport in SiO_2 and hBN-supported graphene devices is shown in Figure 3. References to hBN-supported devices indicate current-annealed, monolayer graphene on five-layer CVD hBN measured at a pressure of 10^{-6} Torr. Graphene devices on SiO_2 were probed in ambient air, under high vacuum (10^{-6} Torr), and after current-annealing. These devices were systematically biased to electrical breakdown once their contact resistance had been extracted, and the measurements were compared with those performed on hBN-supported samples. We find that breakdown characteristics, which reflect high-field performance, depend on vacuum conditions, substrate type, annealing, and channel length. Figure 3c shows a consistent increase in maximum sustained current for 500 nm channel length devices when measured in ambient air, in high vacuum (10^{-6} Torr), post-annealing (10^{-6} Torr), and on a hBN substrate, respectively. These successive improvements are attributed to several factors and will be discussed in the following section. We also observed that devices with shorter channel lengths showed larger breakdown currents (Figure 3d) and higher maximum current densities (Figure 3e), but sustained less power as compared to longer channels (Figure 3f). This is consistent with the expectation that longer channel lengths provide better heat dissipation via a larger graphene-substrate contact area, while shorter channels have fewer total surface impurities limiting carrier scattering, allowing greater sustained current. From the data in Figure 3, we find that annealed, hBN-supported graphene devices under high vacuum exhibited superior high-field performance, with current densities of ~10^9 A/cm^2 (3 mA/μm), three orders of magnitude greater than state-of-the-art copper interconnects,[42] and an order of magnitude increase in sustained power as compared to similar devices under ambient. Performance disparities due to varying vacuum conditions, current-annealing, and substrate engineering are discussed in detail below.

Samples tested under ambient conditions were found to fail earlier (i.e, lower electric field, lower current density, and lower power) than devices measured in vacuum, which is attributed to oxidation at the elevated temperature caused by Joule heating (Figure 3c-f).[43] Oxidation is suppressed for devices under high vacuum, and they sustained twice as much power before electrical breakdown as compared to devices in air (Figure 3f). We attribute device failure primarily to defect formation and growth at contamination and scattering sites. This is supported by the fact that annealed devices consistently showed better high-field performance and greater current/power before electrical breakdown (Figure 3c and Figure 3e), suggesting that adsorbed surface impurities[44] (e.g. water,[45] oxygen,[46] and PMMA,[47] which are known to be removed by Joule heating, act as nuclei for defect formation and accumulation that lead to device breakdown. Furthermore, improved crystallinity resulting from current-annealing is known to enhance transport.[41,48,49] It has been suggested that breakdown of the SiO_2 may account for device failure[50]; however, greater sustained power was observed in annealed devices (Figure 3f), suggesting oxide breakdown is not the limiting factor under these test conditions. Device failure in annealed samples can be ascribed to self-heating effects that originate from the increasing electrical stress at high bias.[51] Finally, we observed that hBN-supported devices showed superior high-field performance, sustaining greater current densities and power to that of similar devices on SiO_2 (Figure 3e and Figure 3f). The performance gains are accredited to hBN's greater thermal conductivity and surface optical phonon modes as compared to SiO_2. A thermal conductivity of 250 W m^{-1} K^{-1} at 300 K was measured for five-layer hBN, over 200 times greater than that of SiO_2[26] while larger optical phonon modes in hBN allow for greater energy absorption at high fields.[20] These properties provide exceptional heat dissipation for the graphene channel, suppressing premature breakdown and contributing to a maximum current density of ~10^9 A/cm^2 (Figure 3e) and sustained power over 200 mW (Figure 3f) in a 500 nm channel, the highest measured for CVD graphene-hBN heterostructures. Electrical breakdown in hBN-supported devices is attributed to excessive Joule heating, which could potentially be mitigated by using an hBN-graphene-hBN stack to allow for greater thermal dissipation. The results thus far provide rational design considerations and potential tradeoffs for future graphene nanoelectronic device fabrication. In brief, record high-field performance was achieved in stacked CVD graphene-hBN heterostructures by utilizing a high vacuum environment, a current annealing process, and an atomically smooth and high thermal conductivity substrate.

Low-field transport data shown in **Figure 4** allow for a comparison of graphene sheet resistivity and mobility in four distinct systems: as-prepared and annealed devices on SiO_2 and five-layer CVD hBN. As-prepared devices on SiO_2 were measured in air while annealed and hBN-supported devices were measured under high vacuum (10^{-6} Torr). At large carrier density ($V_G = V_{Dirac} + 35$ V), as-prepared devices in air exhibited a sheet resistance of ~7 kΩ/η, which was reduced to ~2 kΩ/η by high-vacuum annealing, consistent with the high-temperature vaporization of surface contaminants by Joule heating (Figure 4a). Devices supported on hBN showed even lower sheet resistance of ~0.7 kΩ/η and ~0.4 kΩ/η after annealing (Figure 4a), ascribed to their relative isolation from SiO_2 phonon interactions and dangling bonds/charge traps. The reduction in sheet resistance for the various systems is mirrored in an increase in the measured mobility (Figure 4b). At a density of 5×10^{11} cm^{-2}, the hole and electron carrier mobility is less than 300 cm^2 V^{-1} s^{-1} for devices on SiO_2 under ambient conditions, but increases over

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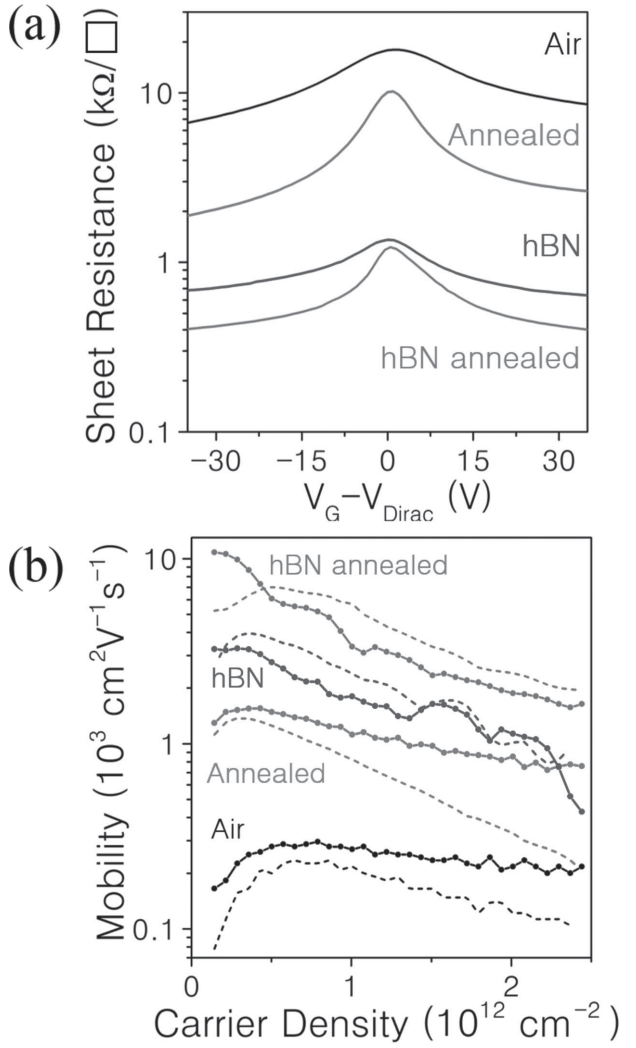

Figure 4. Sheet resistance and mobility. (a) Sheet resistance as a function of gate voltage for graphene devices before/after high-vacuum current-annealing on a SiO_2/five-layer CVD hBN substrate. (b) Hole (solid) and electron (dotted line) mobility as a function of carrier density. Labeling nomenclature is consistent with (a).

an order of magnitude for annealed devices on five-layer hBN (Figure 4b). We report record high hole and electron mobility for CVD hBN-graphene heterostructures, found to exceed 10,000 and 8,000 $cm^2\ V^{-1}\ s^{-1}$, respectively (Figure 4b). Additional information on the derivation of the field-effect mobility using the back-gate configuration is provided in the supporting information.[52] For each type of sample, the mobility reaches a maximum at an intermediate carrier density, as noted in an earlier study.[17] The mobility is suppressed at low carrier density by impurity scattering and at high density due to the increased effect of acoustic phonon scattering.

To summarize, we investigated the transport of CVD graphene on five-layer CVD hBN as a way to explore capabilities to scale high quality graphene devices via substrate engineering. A novel transfer method was utilized to provide low-contamination layer-by-layer stacking to fabricate CVD graphene-hBN heterostructures. Devices were fabricated in the TLM configuration, and high-field transport revealed consistent performance improvements from devices in ambient air, to a high vacuum environment, after current annealing, and finally on hBN substrates. At high-bias, the hBN substrate aided significantly in device cooling, resulting in very high maximum current densities (~10^9 A/cm^2) and sustained power (>200 mW). At low-bias the smooth surface and low density of charge traps associated with the hBN substrate allowed observation of hole and electron carrier mobilities in excess of 8,000 $cm^2\ V^{-1}\ s^{-1}$, the highest measured for CVD graphene-hBN heterostructures, and a sheet resistance of 400 Ω/□. The resulting work provides a pathway towards a scalable method for improving graphene transport properties via substrate engineering applicable in both high- and low-field applications.

Experimental Section

Synthesis: Graphene monolayers were synthesized on 100-μm thick Cu foil (Alfa Aesar, 42189) in a 1 in. tube furnace (Lindberg blue M, TF55035) at atmospheric pressure. The furnace was first heated to 1057 °C for 35 min in a stream of 500 sccm of Ar (*99.999%*) and 50 sccm of H_2 (*99.999%*). After annealing of the Cu foil, H_2 gas flow was reduced to 25 sccm and diluted CH_4 (GTS-WELCO, 1.05% balanced by Ar) was introduced at 2 sccm. Graphene was grown for 100 min before the methane was stopped and the furnace allowed to cool. Hexagonal boron nitride monolayers synthesis followed identical starting procedures as graphene growth however an ammonia borane (AB) source (Sigma-Aldrich, 682098) was introduced into the 1 in. tube furnace. The AB source was placed 15 cm away from the edge of the furnace. After annealing the Cu foil at 1057 °C for 35 min under 500 sccm of Ar and 50 sccm of H_2, the AB source was moved 7 cm towards the Cu foil, and growth was conducted with a reduced H_2 flow rate of 20 sccm. After 15 min, the system was cooled to 1030 °C before the AB source was relocated to its original position. The furnace was rapidly cooled to room temperature in a flow of 1000 sccm of Ar and 10 sccm of H_2.

Fabrication of graphene-hBN heterostructures: A sacrificial layer (MicroChem Corp., 950 PMMA C4) was spin coated on copper foil containing monolayer graphene and gently dried under N_2 for 30 min. The graphene was then released from the copper foil using the bubbling transfer method[28] and transported from the ionic solution using a polyethylene therepthalate (PET) substrate to three consecutive deionized water baths. The PMMA-graphene sample was then scooped onto the surface of a hBN-copper foil sample synthesized as outlined above. The PMMA-graphene-hBN-Cu foil stack was allowed dry for 40 min at an incline. Repeated identical bubbling transfer steps were used to allow additional hBN layers to be stacked beneath the original structure. After the final bubbling transfer of the desired PMMA-graphene-multilayer-hBN stack, the heterostructure was scooped onto a SiO_2/Si substrate and allowed to dry at an incline for 30 min. The wafer was coated with PMMA to allow the original scaffolding layer to soften and then dried for 20 min. The PMMA was removed with gentle acetone rinsing for 10 min and submerged in an acetone bath for 7 min. The chip was rinsed with Isopropanol for 3 min and dried with compressed N_2 gas.

Fabrication of devices: Positive tone electron beam resist (MicroChem Corp., 950 PMMA C4) was spin-coated onto the

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graphene-hBN chip and baked at 170 °C for 1 min. Ebeam lithography was used to pattern a TLM structure in the resist and a 3 nm Cr/40 nm Au metallization layer was deposited using a home built thermal evaporator followed by liftoff. Using the same resist, a second round of ebeam lithography was used to define a 3-μm wide etch mask that was patterned above the TLM electrodes (see Figure S2 in Supplementary Information). The chip was etched in O_2 plasma for 30 seconds at 40 W (Technics PE II-A) to isolate a graphene ribbon that spanned the TLM electrodes (Figure 2a); the bulk of the silicon substrate was used as the backgate electrode. A final liftoff completed device fabrication. Identical steps were used to fabricate graphene devices on SiO_2.

Sample Characterization: Scanning electron micrographs (FEI Strata DB235) were taken with 5 kV beam voltage. For Raman spectroscopy and mapping, an excitation laser of 532 nm wavelength was used. Atomic force micrographs (Asylum MFP-3D) of hBN on SiO_2/Si (300 nm oxide) were taken with tapping mode. Transmission electron microscopy, electron diffraction, and high resolution imaging were carried out in a JEOL 2010, a JEOL 2010F, and a FEI Titan operating at 200, 200, and 300 kV, respectively. Graphene devices were electrically probed using a Lakeshore probe station that allowed for high vacuum (10^{-6} Torr) measurements. A National Instruments 6221 DAQ card was used to sources the bias voltage and a preamplifier was used to read the current. A Keithley 5417A multimeter was used to supply the gate voltage. A custom Labview program is used to set/sweep the bias and gate voltages in addition to electrical measurements.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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